

FWS-7400

Network Appliance

User's Manual 2nd Ed

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Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● FWS-7400	1
● EAR bracket kit	1
● Console cable	1
● Product DVD	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. All cables and adapters supplied by AAEON are certified and in accordance with the material safety laws and regulations of the country of sale. Do not use any cables or adapters not supplied by AAEON to prevent system malfunction or fires.
3. Make sure the power source matches the power rating of the device.
4. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
5. Always completely disconnect the power before working on the system's hardware.
6. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
7. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
8. Always disconnect this device from any AC supply before cleaning.
9. While cleaning, use a damp cloth instead of liquid or spray detergents.
10. Make sure the device is installed near a power outlet and is easily accessible.
11. Keep this device away from humidity.
12. Place the device on a solid surface during installation to prevent falls
13. Do not cover the openings on the device to ensure optimal heat dissipation.
14. Watch out for high temperatures when the system is running.
15. Do not touch the heat sink or heat spreader when the system is running
16. Never pour any liquid into the openings. This could cause fire or electric shock.

17. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.
18. If any of the following situations arises, please the contact our service personnel:
 - i. Damaged power cord or plug
 - ii. Liquid intrusion to the device
 - iii. Exposure to moisture
 - iv. Device is not working as expected or in a manner as described in this manual
 - v. The device is dropped or damaged
 - vi. Any obvious signs of damage displayed on the device
19. **DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.**

Warning!



This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte. Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur. Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON Embedded Box PC/ Industrial System

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板 及其电子组件	○	○	○	○	○	○
外部信号 连接器及线材	○	○	○	○	○	○
外壳	○	○	○	○	○	○
中央处理器 与内存	○	○	○	○	○	○
硬盘	○	○	○	○	○	○
电源	○	○	○	○	○	○
<p>O: 表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。</p> <p>X: 表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。</p> <p>备注： 一、此产品所标示之环保使用期限，系指在一般正常使用状况下。 二、上述部件物质中央处理器、内存、硬盘、光驱、触控模块为选购品。</p>						

China RoHS Requirement (EN)

Poisonous or Hazardous Substances or Elements in Products
AAEON Embedded Box PC/ Industrial System

Component	Poisonous or Hazardous Substances or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
PCB & Other Components	○	○	○	○	○	○
Wires & Connectors for External Connections	○	○	○	○	○	○
Chassis	○	○	○	○	○	○
CPU & RAM	○	○	○	○	○	○
Hard Disk	○	○	○	○	○	○
PSU	○	○	○	○	○	○

O: The quantity of poisonous or hazardous substances or elements found in each of the component's parts is below the SJ/T 11363-2006-stipulated requirement.

X: The quantity of poisonous or hazardous substances or elements found in at least one of the component's parts is beyond the SJ/T 11363-2006-stipulated requirement.

Note: The Environment Friendly Use Period as labeled on this product is applicable under normal usage only

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Chapter 1

Product Specifications

1.1 Specifications

System

- **Processor** Intel® 4th generation Core™ Processor
- **System Memory** 240-pin Dual-Channel DDR3 1333/1600 DIMM
Socket x 2, up to 16 GB
- **Chipset** Intel® H81
- **Ethernet** Intel® 82583L controller, Gigabit Ethernet x 6
(optional up to 2 pairs LAN bypass function)
- **BIOS** AMI BIOS ROM
- **Serial ATA** SATA 6.0 Gb/s x 2 (optional 3 SATA ports)
- **SSD** -
- **Expansion Interface** Network Interface Module (NIM) x 1 (optional);
PCI-E[x8] slot x 1
- **Watchdog Timer** 1~255 steps by software programming
- **RTC** Internal RTC
- **Storage** 3.5" SATA HDD bay x 1 or
2.5" SATA HDD bay x 2
- **Front Panel I/O** Power LED x 1
Bypass LED x 2 (Optional)
Status LED x 1
HDD Active LED x 1
USB port x 2
RJ-45 port with LED x 6
RJ-45 console x 1
LCM Display and 4 keypad x 1

- **Rear Panel I/O**
 - Software programming switch x 1
 - AC power input x 1
 - Power switch x 1
 - Expansion slot x 2 (optional PCI-E[x8] slot x 1)
- **Color**
 - Black
- **Power Supply**
 - Flex ATX 250W
- **Dimension (W x D x H)**
 - 430 x 44 x 305 mm (16.9 x 1.73 x 12.01")

Graphics

- **Chipset**
 -
- **Graphic Engine**
 -
- **Resolution**
 -
- **Output Interface**
 - Pin header reserved for Graphic display

I/O

- **Serial Port**
 - RJ-45 console x 1 (on front panel)
 - RS-232 box header x 1 (optional)
- **Keyboard and Mouse**
 - Reserved pin header (optional)
- **USB**
 - USB3.0 x 2
 - USB2.0 x 2 (Optional Pin Header)

Environmental

- **Operating Temperature**
 - 0~40°C (32~104°F)
- **Storage Temperature**
 - 20 ~60°C (-4 ~140°F)
- **Operating Humidity**
 - 10%~80% relative humidity, non-condensing

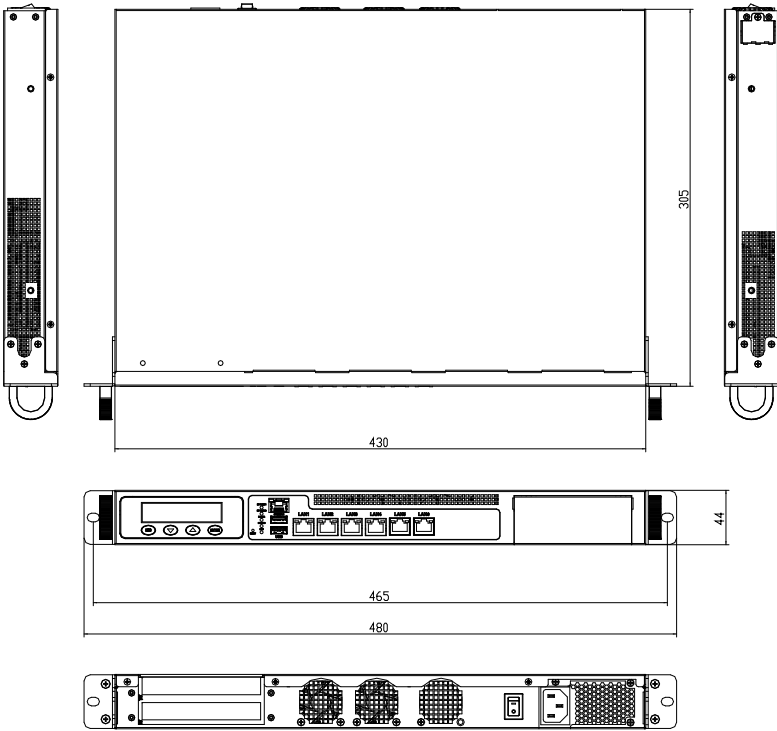
- **Storage Humidity** 10~80% @ 40°C, non-condensing
- **Anti-Vibration** 0.5 Grms/5~500Hz/ operation (3.5"Hard Disk Drive)
1.5 Grms/5~500Hz/ non-operation
- **Anti-Shock** 10G peak acceleration (11m sec. duration), operation
20G peak acceleration (11m sec. duration), non operation

Chapter 2

Hardware Information

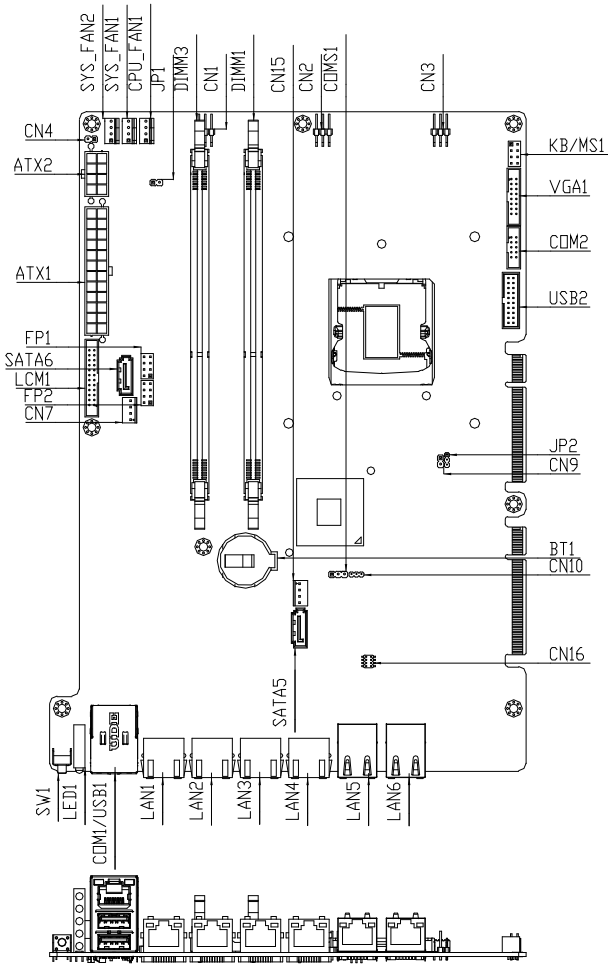
2.1 Dimensions

System

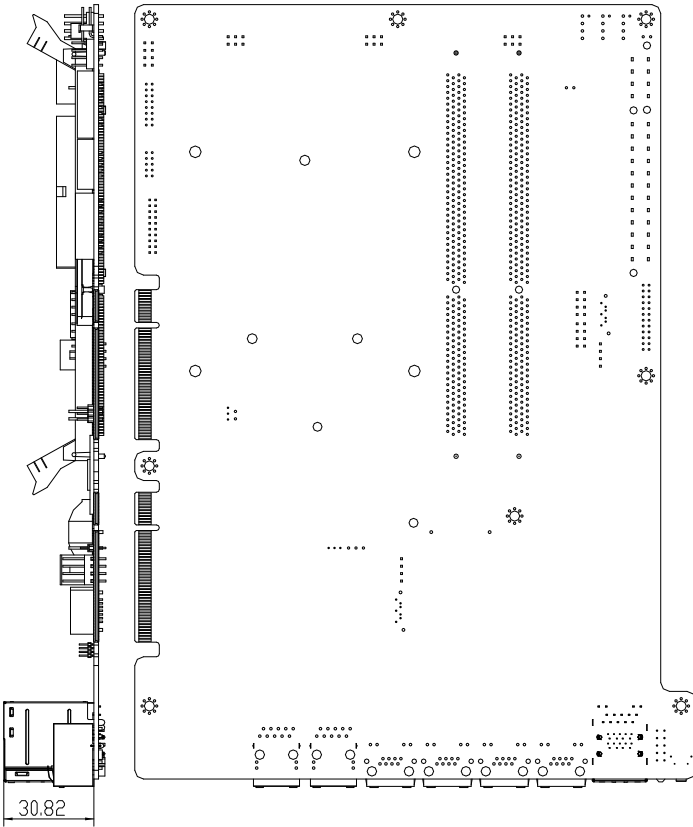


2.2 Jumpers and Connectors

Component Side



Solder Side

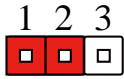


2.3 List of Jumpers

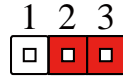
Please refer to the table below for all of the board's jumpers that you can configure for your application

Label	Function
JP2	Auto Power Button
CMOS	Clear CMOS

2.3.1 Clear CMOS (CMOS)

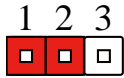


Protected (Default)

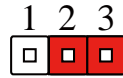


Clear CMOS

2.3.2 Auto PWRBTN Selection (JP2)



Power ON by Button (Default)



Auto Power ON

2.4 List of Connectors

Please refer to the table below for all of the board's connectors that you can configure for your application

Label	Function
FP1	Front Panel Connector 1
FP2	Front Panel Connector 2
KB/MS1	PS2 KB/MS Pin Header
VGA1	VGA Pin Header
COM2	RS-232 Pin Header
USB2	USB 3.0 Pin Header
DIMM1	DDR3 DIMM Slot
DIMM2	DDR3 DIMM Slot
DIMM3	DDR3 DIMM Slot
DIMM4	DDR3 DIMM Slot
BT1	Battery
SATA1~SATA6	SATA Connector
LAN1	10/100/1000 Base Ethernet Connector
LAN2	10/100/1000 Base Ethernet Connector
LAN3	10/100/1000 Base Ethernet Connector
LAN4	10/100/1000 Base Ethernet Connector
LAN5	10/100/1000 Base Ethernet Connector
LAN6	10/100/1000 Base Ethernet Connector
LAN7	10/100/1000 Base Ethernet Connector
LAN8	10/100/1000 Base Ethernet Connector
CPU_FAN1	4 Pin Fan Connector
SYS_FAN1	4 Pin Fan Connector
SYS_FAN2	4 Pin Fan Connector

Label	Function
CN7	SATA Power Connector
CN11~CN15	SATA Power Connector
CN4	Power Bottom
LCM1	LCM Connector
ATX1	24Pin ATX Power Connector
ATX2	8Pin ATX Power Connector
COM1/USB1	COM/USB3 Connector

2.4.1 Front Panel Connector (FP1)

Pin	Signal	Pin	Signal
1	External Speaker (+)	2	Key Board Lock (+)
3	NC	4	GND
5	Internal Buzzer (-)	6	I2C Bus SMB Clock
7	External Speaker (-)	8	I2C Bus SMB Data

*Close Pin 5, 7 to enable internal buzzer

2.4.2 Front Panel Connector (FP2)

Pin	Signal	Pin	Signal
1	Power On Button (+)	2	Reset Switch (+)
3	Power On Button (-)	4	Reset Switch (-)
5	HDD LED (+)	6	Power LED (+)
7	HDD LED (-)	8	Power LED (-)

2.4.3 USB2.0 Port PIN Header (USB2)

Pin	Signal	Pin	Signal
1	VCC	20	NC
2	NC	19	VCC
3	NC	18	NC
4	GND	17	NC

5	NC	16	GND
6	NC	15	NC
7	GND	14	NC
8	USBP_ON_C	13	GND
9	USBP_OP_C	12	USBP_1N_C
10	NC	11	USBP_1P_C

2.4.4 COM Port Connector (COM2)

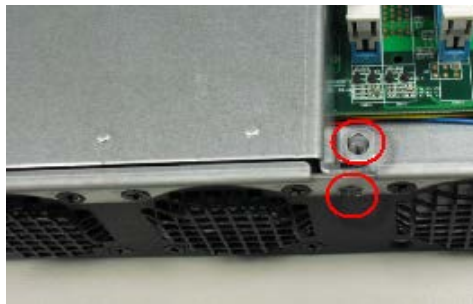
Pin	Signal	Pin	Signal
1	DCD2X	2	SIN2X
3	SOUT2X	4	DTR2X
5	GND	6	DSR2X
7	RTS2X	8	CTS2X
9	RI2X	10	NC

2.4.5 KB/MS Connector (KB/MS1)

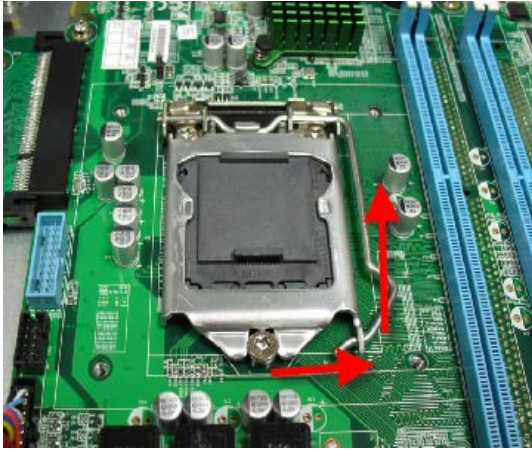
Pin	Signal	Pin	Signal
1	KBDATA	2	KBCLK
3	GND	4	+5V_KB
5	MSDATA	6	MSCLK
7	NC		

2.5 Installing the CPU and the Heat Sink

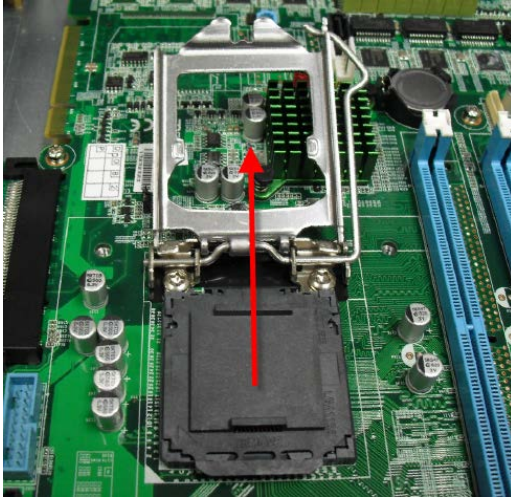
1. Loosen the screws and remove the fan duct



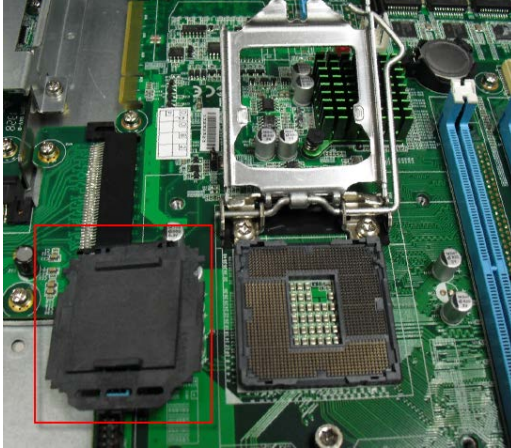
2. Release the lock pole of the CPU bracket



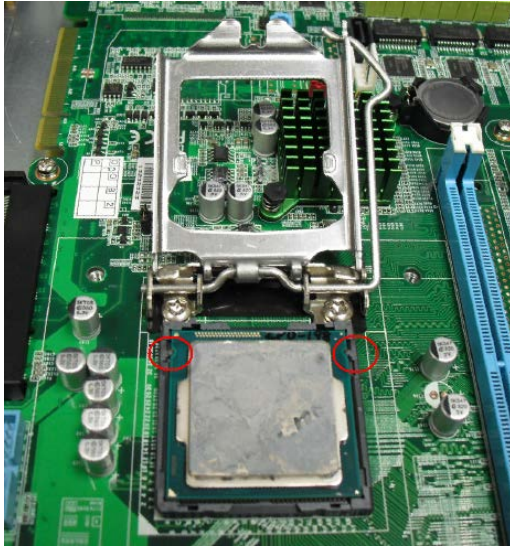
3. Remove the four highlighted screws to remove the HDD bracket



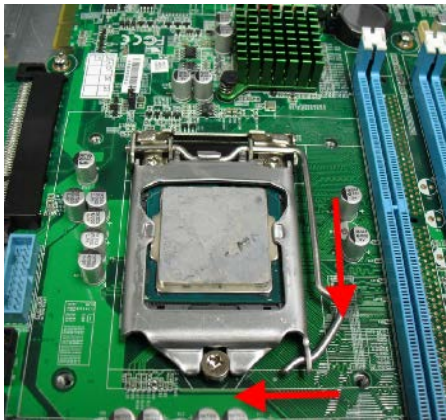
4. Lift up the CPU cover



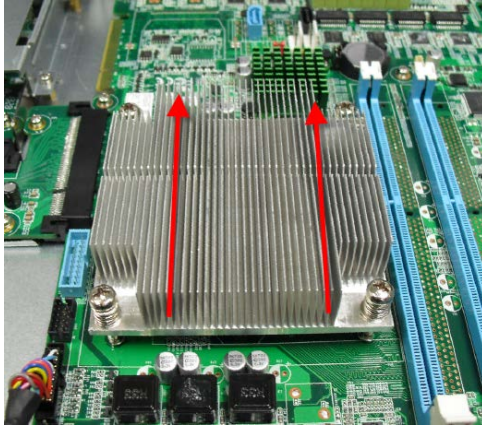
5. Place the CPU to the socket and have the two fillisters locked properly



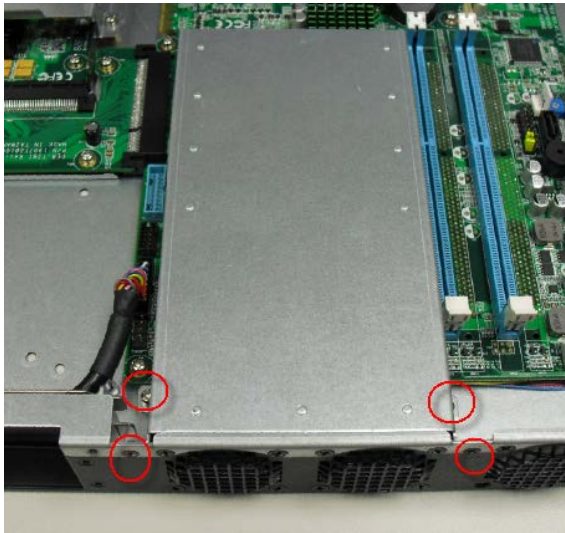
6. Close the CPU bracket and lock the pole to the position



7. Cover the Heatsink on the CPU and watch out the direction of the Heatsink that did not against the airflow



8. Fasten the four screws to lock the air duct

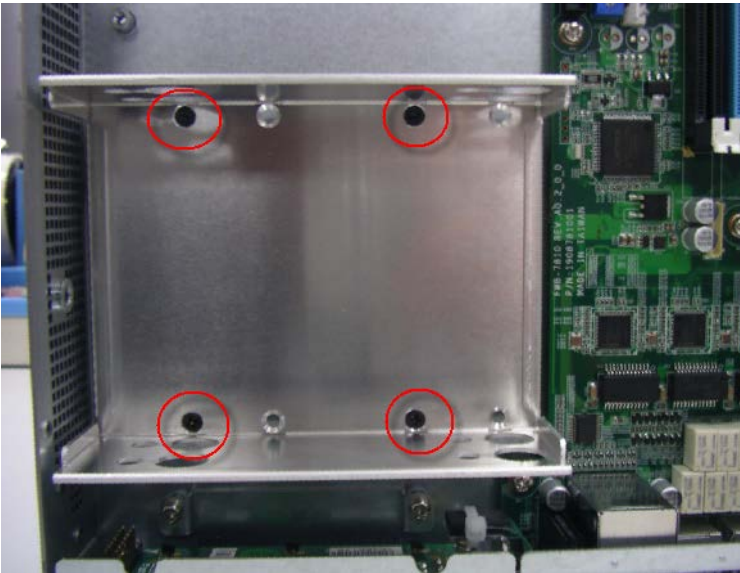


2.6 Installing the Two 2.5" Hard Disk Drive (HDD)

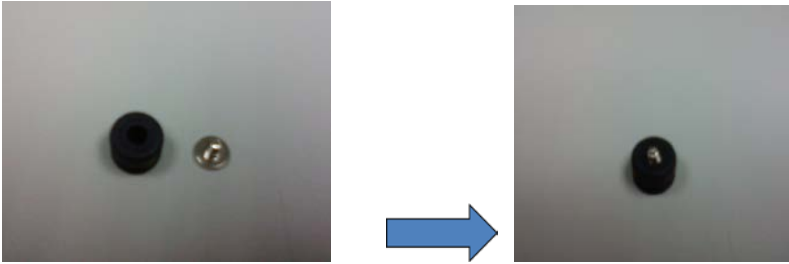
1. Unscrew the upper lid



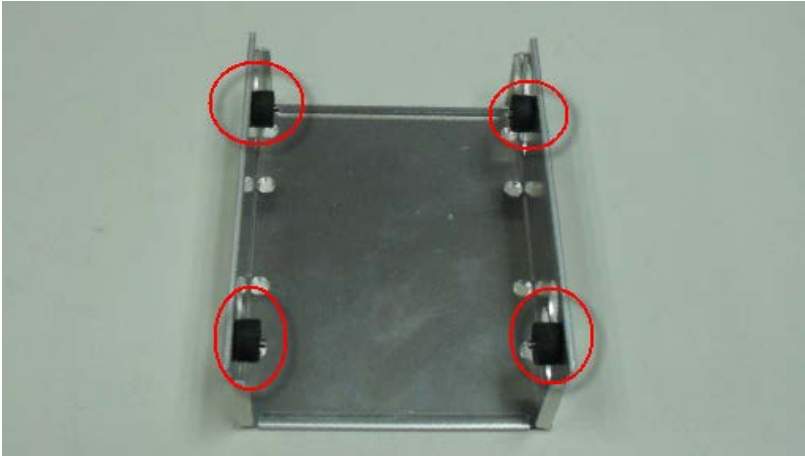
2. Unfasten the four screws



3. put the screw into cushion



4. put the assembled cushions to the upper place of the 2.5" HDD bracket



- put the assembled cushions to the lower place of the 2.5" HDD bracket



- Lock the HDD to the lower cushions with four screws



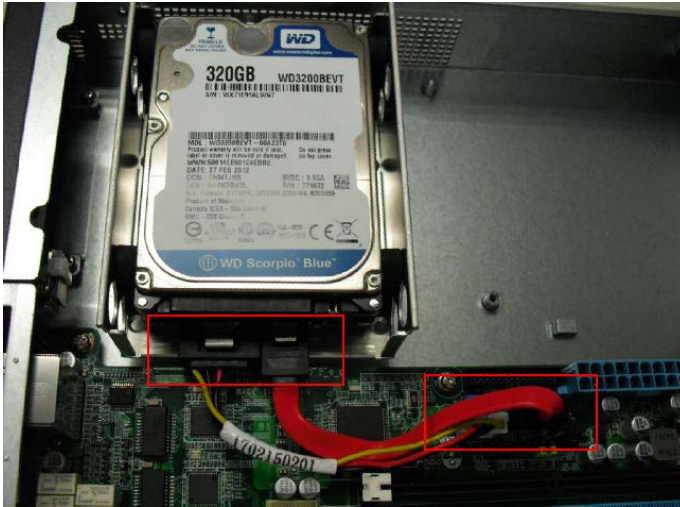
- Lock the second HDD to the upper cushions with four screws



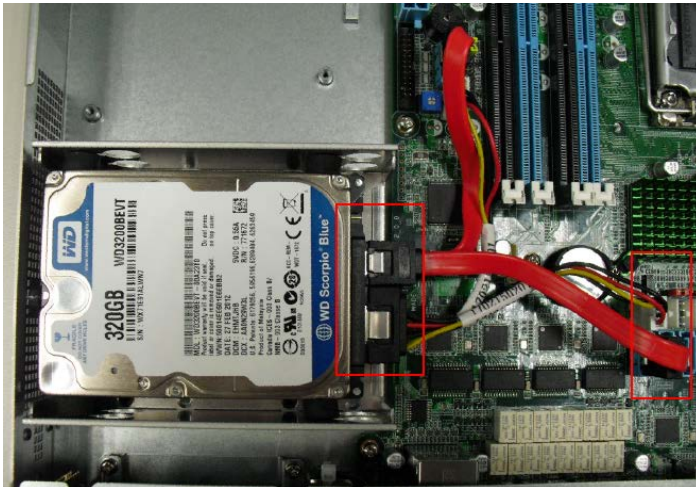
- Lock the HDD bracket to the chassis with four screws



9. Connect the SATA cable and power cable to the HDD in lower place



10. Connect the SATA cable and power cable to the HDD in upper place



Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

The system uses certain routines to perform testing and initialization. If an error, fatal or non-fatal, is encountered, a few short beeps or an error message will be outputted. The board can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory. If they do not match, an error message will be outputted, in which case you will need to run the BIOS setup program to set the configuration information in memory.

There are three situations in which you will need to change the CMOS settings:

- You are starting your system for the first time
- You have changed your system's hardware
- The CMOS memory has lost power and the configuration information is erased

The system's CMOS memory uses a backup battery for data retention, which is to be replaced once emptied.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press or <F2> immediately while your computer is powering up.

The function for each interface can be found below.

Main – Date and time can be set here. Press <Tab> to switch between date elements

Advanced – Advanced setup parameters

Chipset – For hosting bridge parameters

Boot – Enable/ Disable quiet Boot Option

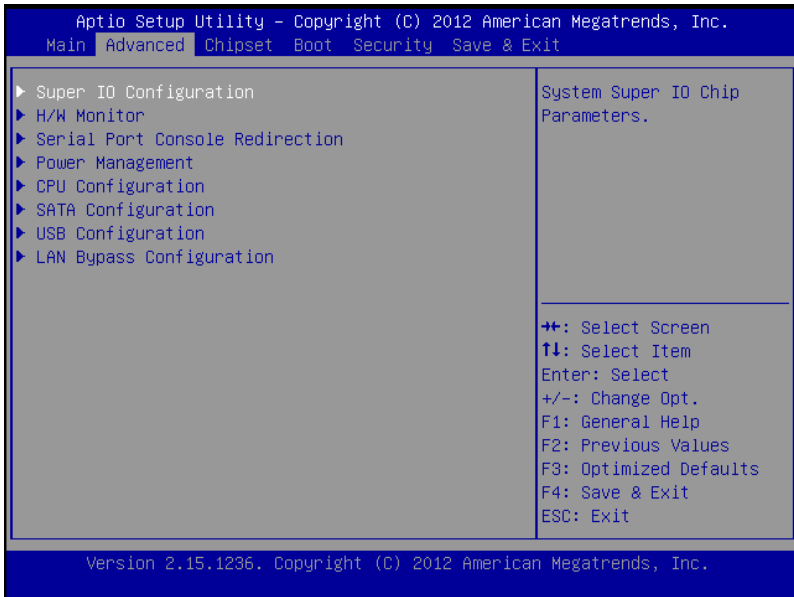
Security – The setup administrator password can be set here

Save & Exit – Save your changes and exit the program

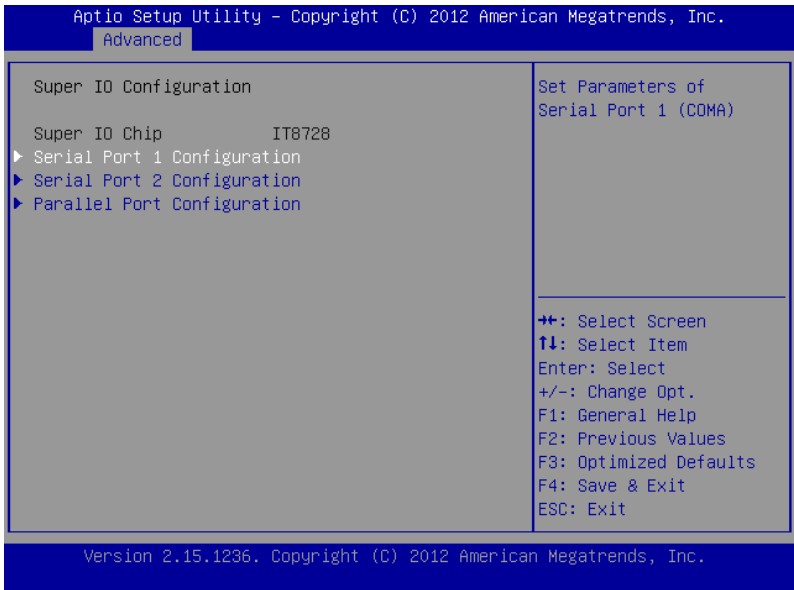
3.3 Setup Submenu: Main



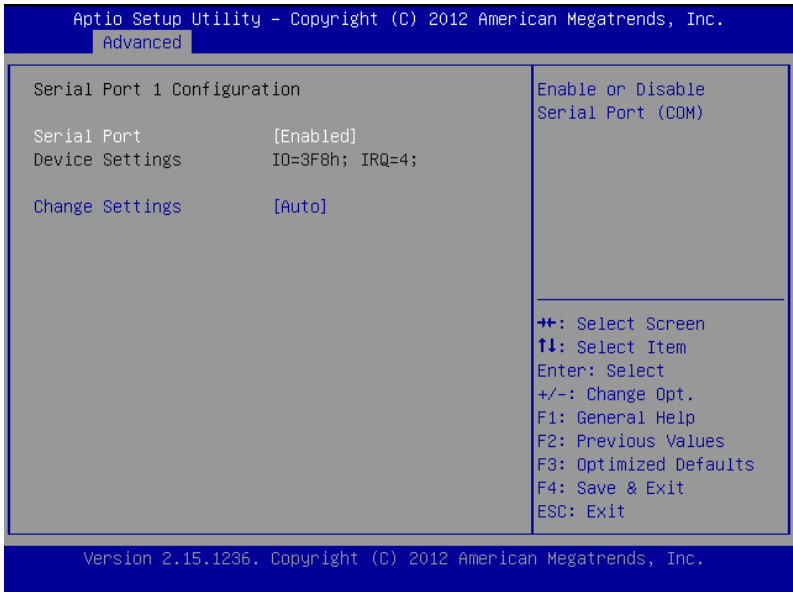
3.4 Setup Submenu: Advanced



3.4.1 Advanced: Super IO Configuration



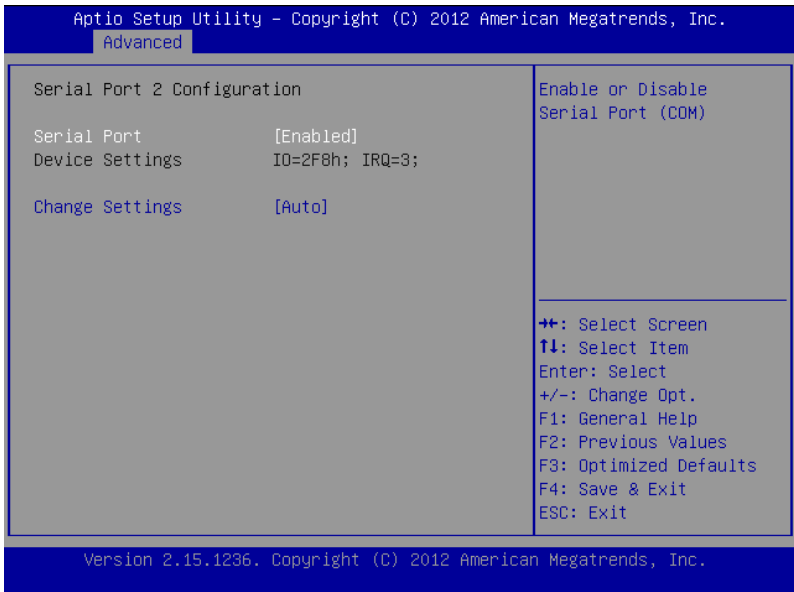
3.4.1.1 Super IO Configuration: Serial Port 1 Configuration



Options summary:

Serial Port	Disabled
	Enabled
Enable or Disable Serial Port (COM)	
Serial Port	Auto
	IO=3F8h; IRQ=4;
	IO=3F8h; IRQ=3,4,5,6,7,9,10,11,12;
	IO=2F8h; IRQ=3,4,5,6,7,9,10,11,12;
	IO=3E8h; IRQ=3,4,5,6,7,9,10,11,12;
	IO=2E8h; IRQ=3,4,5,6,7,9,10,11,12;
Select an optimal setting for Super IO device.	

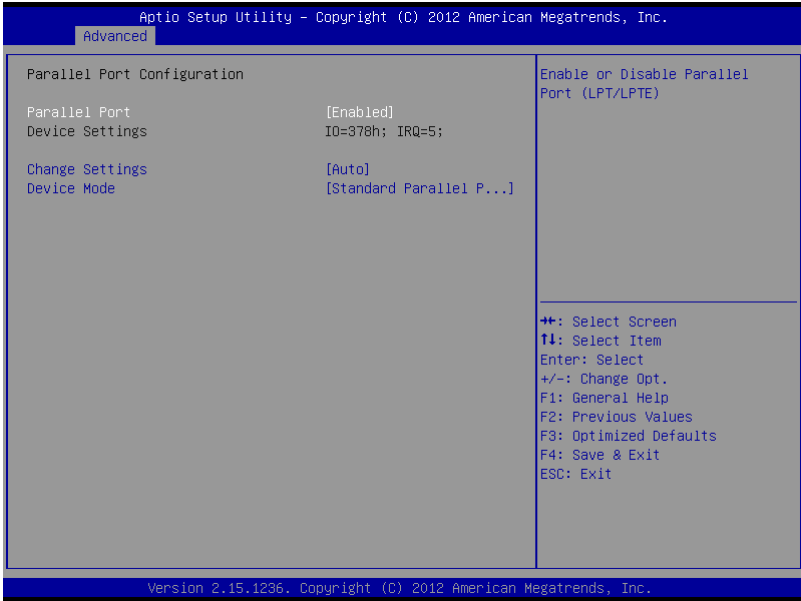
3.4.1.2 Super IO Configuration: Serial Port 2 Configuration



Options summary:

Serial Port	Disabled
	Enabled
Enable or Disable Serial Port (COM)	
Serial Port	Auto
	IO=2F8h; IRQ=3;
	IO=3F8h; IRQ=3,4,5,6,7,9,10,11,12;
	IO=2F8h; IRQ=3,4,5,6,7,9,10,11,12;
	IO=3E8h; IRQ=3,4,5,6,7,9,10,11,12;
	IO=2E8h; IRQ=3,4,5,6,7,9,10,11,12;
Select an optimal setting for Super IO device.	

3.4.1.3 Super IO Configuration: Parallel Port Configuration

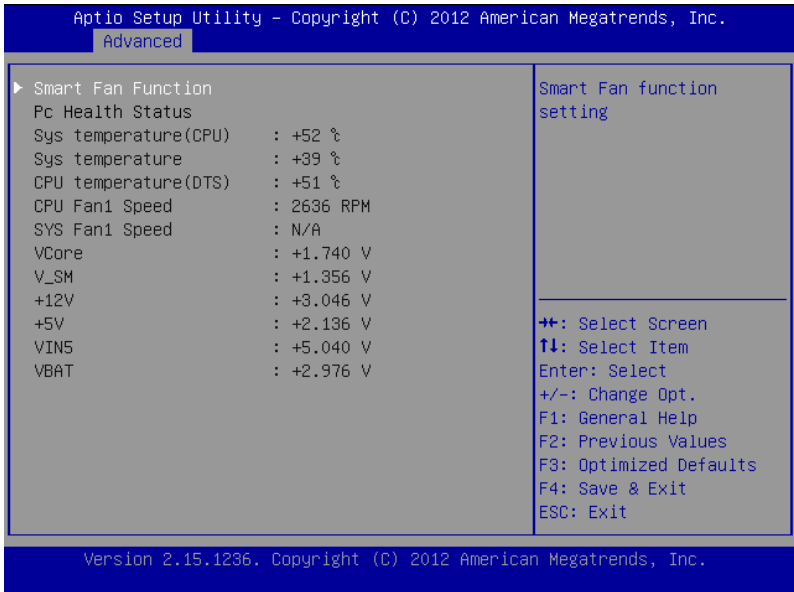


Options summary:

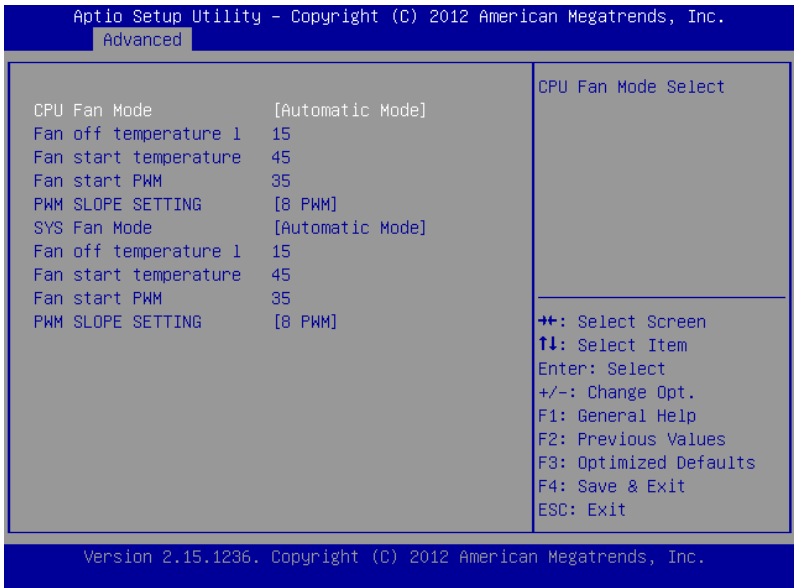
Parallel Port	Disabled
	Enabled
Enable or Disable Serial Port (COM)	
Change Settings	Auto
	IO=378h; IRQ=5;
	IO=378h; IRQ=5,6,7,9,10,11,12;
	IO=278h; IRQ=5,6,7,9,10,11,12;
IO=3BCh;IRQ=5,6,7,9,10,11,12;	
Select an optimal setting for Supeer IO device.	
Device Mode	Standard Parallel Port Mode
	EPP Mode

	ECP Mode
	EPP Mode & ECP Mode
Change the Printer Port mode.	

3.4.2 Advanced: H/W monitor



3.4.2.1 H/W monitor: Smart Fan Function

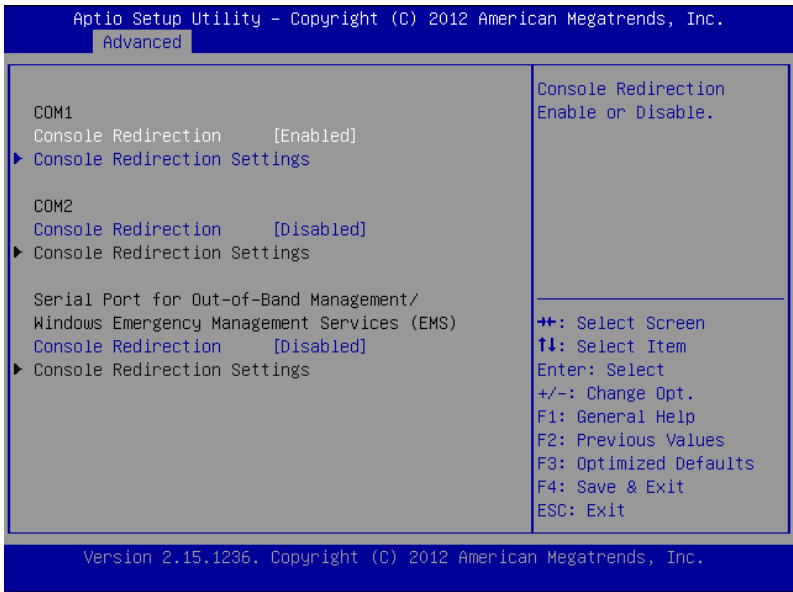


Options summary:

Smart Fan Mode	Full on Mode
	Automatic Mode
	Manual Mode
Smart Fan Mode Select	
Fan off temperature limit	15 (0-127)
Fan will of when temperature lower than this limit.	
Fan start temperature limit	45 (0-127)
Fan will work when temperature higher than this limit.	
Fan start PWM	35 (0-255)
Fan will start with this PWM value(Range 0-255).	
PWM SLOPE SETTING	0.125 PWM
	0.25 PWM

	0.5 PWM
	1 PWM
	2 PWM
	4 PWM
	8 PWM
	15.875 PWM
PWM SLOPE Selection	

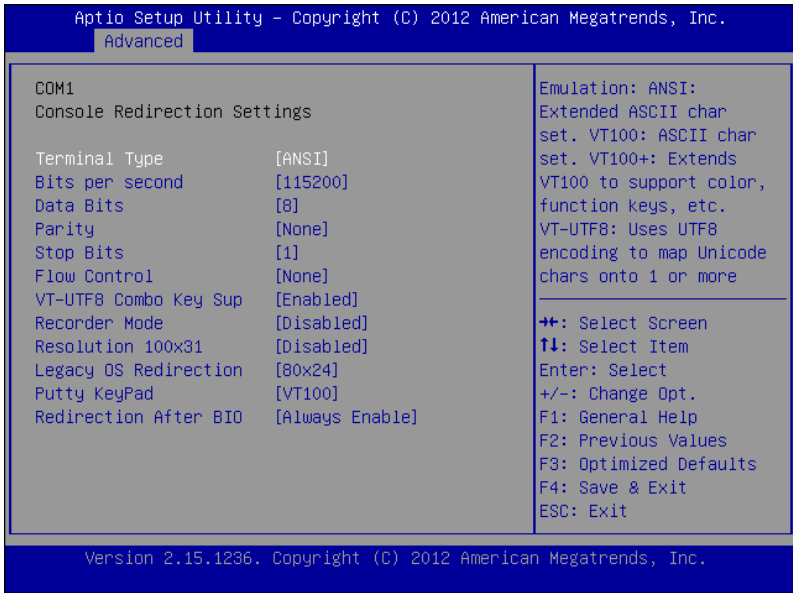
3.4.3 Advanced: Serial Port Console Redirection



Options summary:

Console Redirection	Disabled (COM2)
	Enabled (COM1)
Console Redirection Enabled or Disabled.	

3.4.3.1 Serial Port Console Redirection: Console Redirection Settings



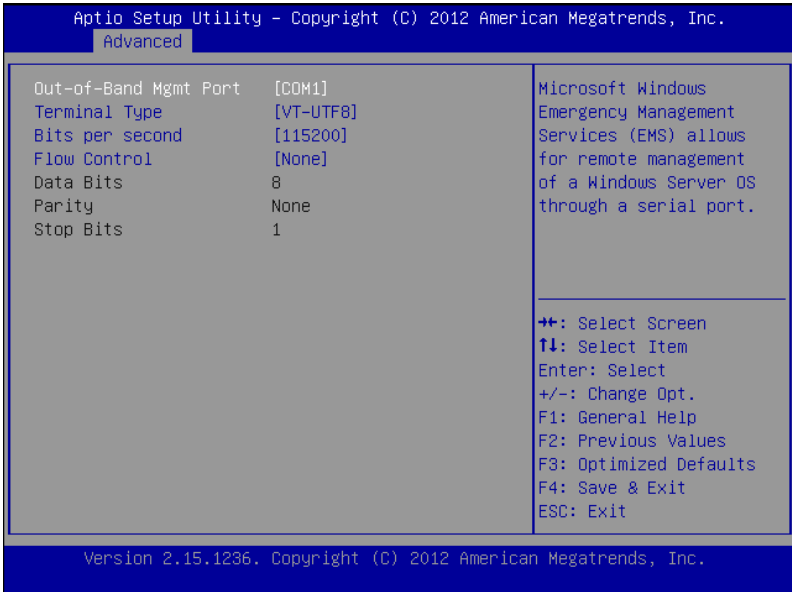
Options summary:

Terminal Type	VT100
	VT100+
	VT-UTF8
	ANSI
Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.	
Bits per second	9600
	19200
	38400
	57600

	115200
Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.	
Data Bits	7
	8
Data Bits	
Parity	None
	Even
	Odd
	Mark
	Space
A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection.	
Stop Bits	1
	2
Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.	
Flow Control	None
	Hardware RTS/CTS
Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.	
VT-UTF8 Combo Key Support	Disabled
	Enabled

Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals	
Recorder Mode	Disabled
	Enabled
On this mode enabled only text will be send. This is to capture Terminal data.	
Resolution 100x31	Disabled
	Enabled
Enables or disables extended terminal resolution	
Legacy OS Redirection Resolution	80x24
	80x25
On Legacy OS, the Number of Rows and Columns supported redirection	
Putty KeyPad	VT100
	LINUX
	XTERMR6
	SCO
	ESCN
	VT400
Select FunctionKey and KeyPad on Putty.	
Redirection After BIOS POST	Always Enable
	BootLoader
The Setting Specify if BootLoader is selected than Legacy console redirection is disabled before booting to Legacy OS. Default value is Always Enable which means Legacy console Redirection is enabled for Legacy OS.	

3.4.3.1 Serial Port Console Redirection: Serial Port for Out-of-Band Management/Windows Emergency Management Services(EMS)



Options summary:

Out-of Band Mgmt Port	COM1
	COM2
Microsoft Windows Emergency Management Services(EMS) allows for remote management of a windows server OS through a serial port.	
Terminal Type	VT100
	VT100+
	VT-UTF8
	ANSI

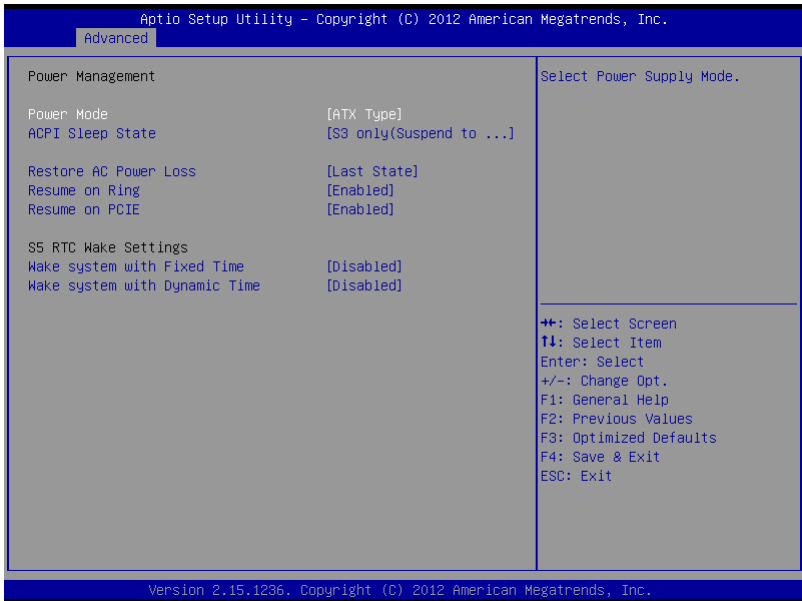
Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.	
Bits per second	9600
	19200
	57600
	115200
Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.	
Flow Control	None
	Hardware RTS/CTS
	Software Xon/Xoff
Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.	
Data Bits	7
	8
Data Bits	
Parity	None
	Even
	Odd
	Mark
	Space

A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection.

Stop Bits	1
	2

Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.

3.4.4 Advanced: Power Management

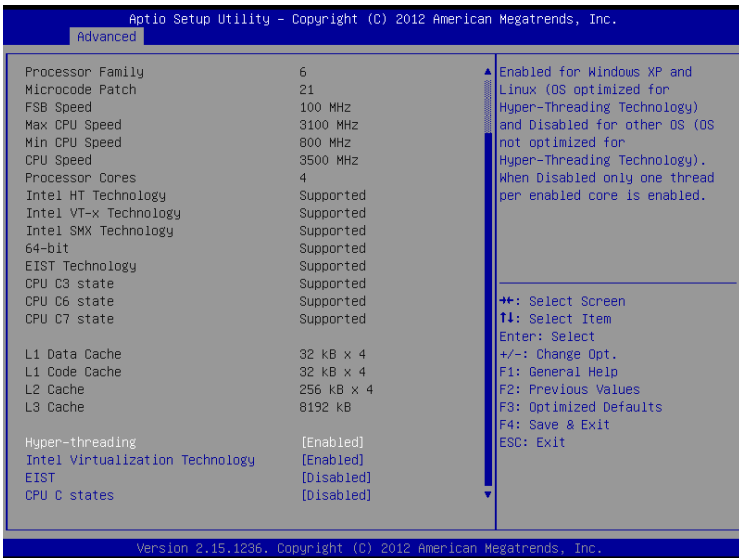
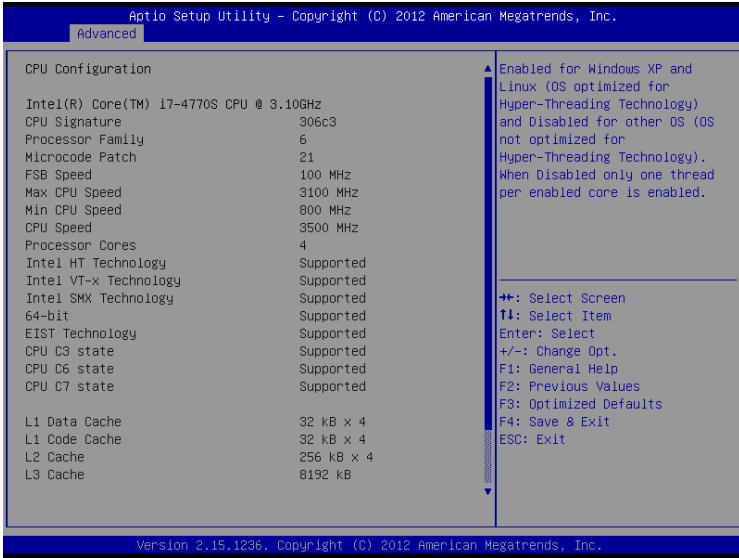


Options summary:

Power Mode	ATX Type
	AT Type
Select Power Supply Mode.	
ACPI Sleep State	Suspend Disabled
	S3 only (Suspend to RAM)
Select ACPI sleep state the system will enter when the SUSPEND button is pressed.	
Restore AC Power Loss	Power Off
	Power On
	Last State
Select AC power state when power is re-applied after a power failure.	
Resume on Ring	Disabled

	Enabled
Enable/Disable Resume from RI# signal.	
Resume on PCIE	Disabled
	Enabled
Enable/Disable Resume from PCIE signal.	
Wake system with Fixed Time	Disabled
	Enabled
Enable or disable System wake on alarm event. When enable, System will wake on the hr::min::sec specified.	
Wake up day	0
Select 0 for daily system wake up, 1-31 for which day of month that you would like the system to wake up.	
Wake up hour	0
Select 0-23 For example enter 3 for 3am and 15 for 3pm.	
Wake up minute	0
0-59	
Wake up second	0
0-59	
Wake system with Dynamic Time	Disabled
	Enabled
Enable or disable System wake on alarm event. When enabled, System will wake on the current time + Increase minute(s).	
Wake up minute increase	1
1-5	

3.4.5 Advanced: CPU Configuration



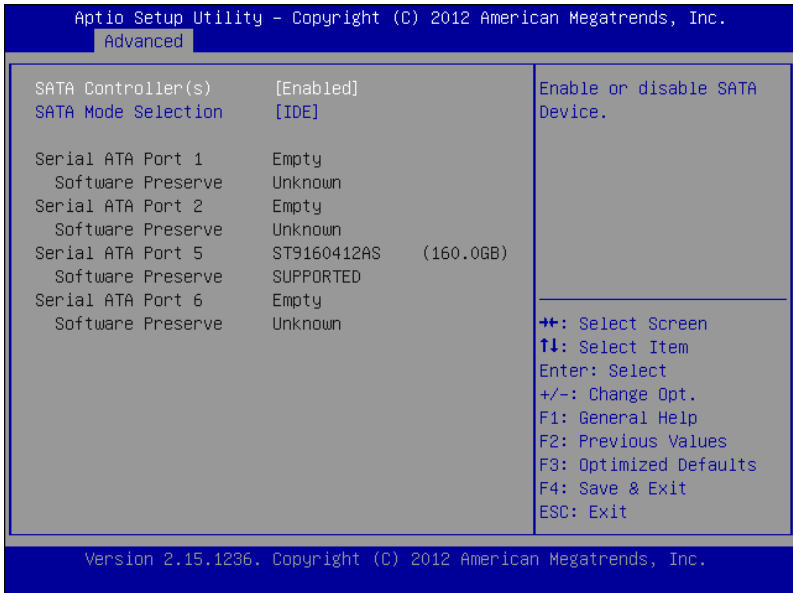
Options summary:

Hyper-threading	Disabled
-----------------	----------

	Enabled
<p>Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology). When Disabled only one thread per enabled core is enabled.</p>	
Intel Virtualization Technology	Disabled
	Enabled
<p>When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.</p>	
EIST	Disabled
	Enabled
Enable/Disable Intel SpeedStep	
CPU C states	Disabled
	Enabled
Enable or disable CPU C states	

3.4.6 Advanced: SATA Configuration

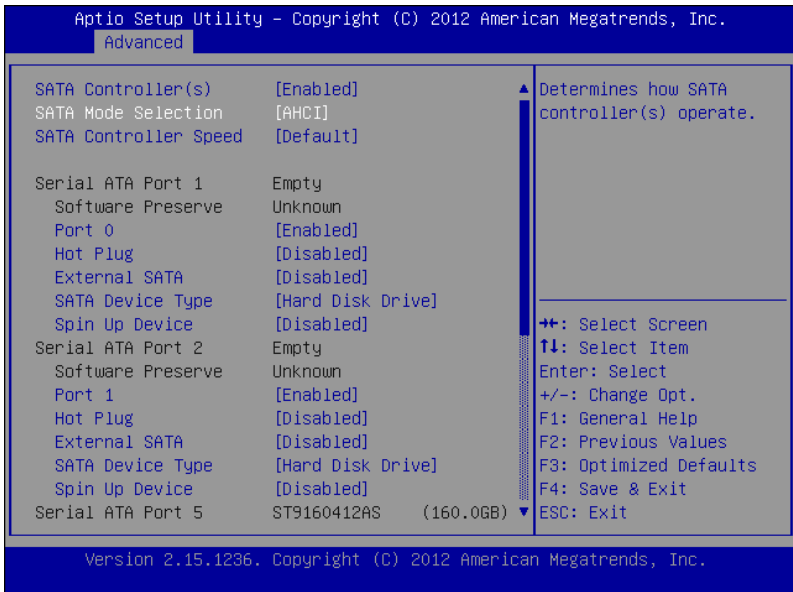
3.4.6.1 SATA Configuration: SATA Configuration (IDE)



Options summary:

SATA Controller(s)	Disabled
	Enabled
Enable or disable SATA Device.	
SATA Mode Selection	IDE
	AHCI
Determines how SATA controller(s) operate.	

3.4.6.2 SATA Configuration: SATA Configuration (AHCI)

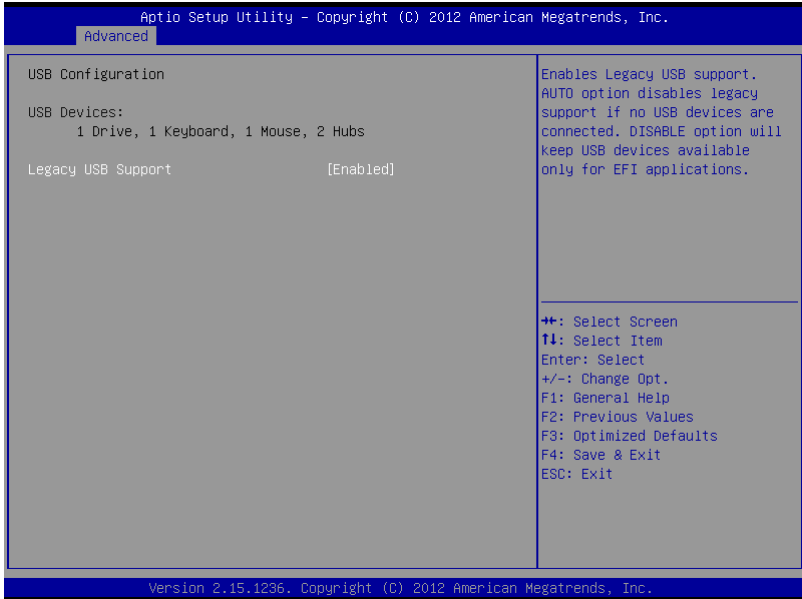


Options summary:

SATA Controller Speed	Disabled
	Enabled
Enable or disable SATA Device.	
SATA Mode Selection	Default
	Gen1
	Gen2
	Gen3
Indicates the maximum speed the SATA controller can support.	
Port	Disabled
	Enabled
Enable or Disable SATA Port	

Hot Plug	Disabled
	Enabled
Designates this port as Hot Pluggable.	
External SATA	Disabled
	Enabled
External SATA Support.	
SATA Device Type	Hard Disk Drive
	Solid State Drive
Identify the SATA port is connected to Solid State Drive or Hard Disk Drive.	
Spin Up Device	Disabled
	Enabled
On an edge detect from 0 to 1, the PCH starts a COMRESET initialization sequence to device.	

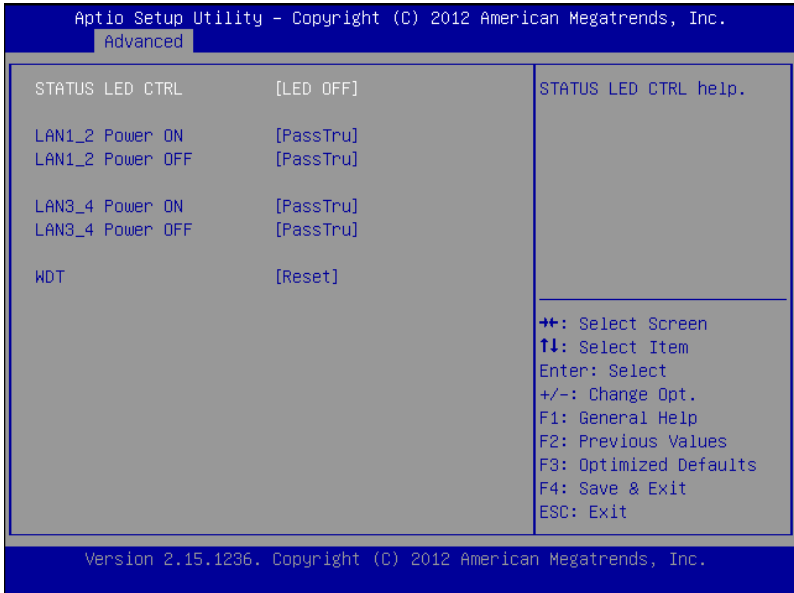
3.4.7 Advanced: USB Configuration



Options summary:

Legacy USB Support	Enabled
	Disabled
	Auto
Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB device available only for EFI applications.	

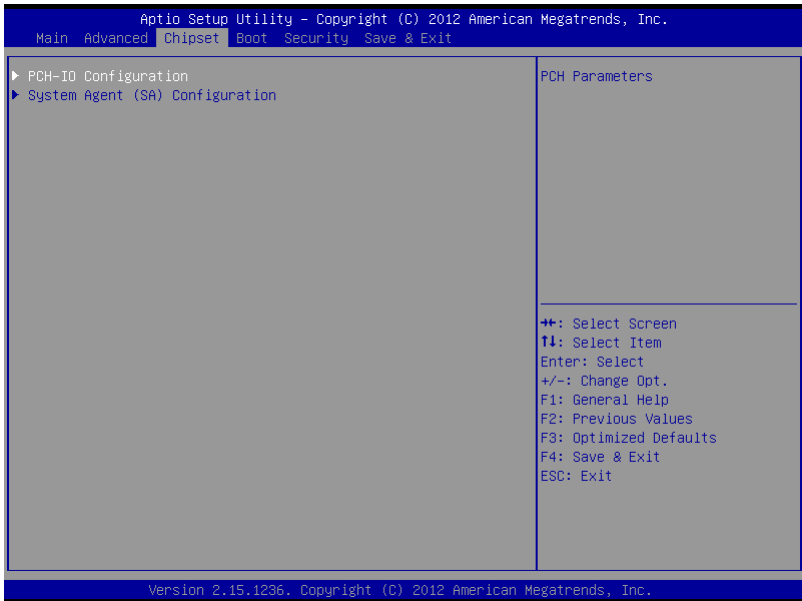
3.4.8 Advanced: LAN Bypass Configuration



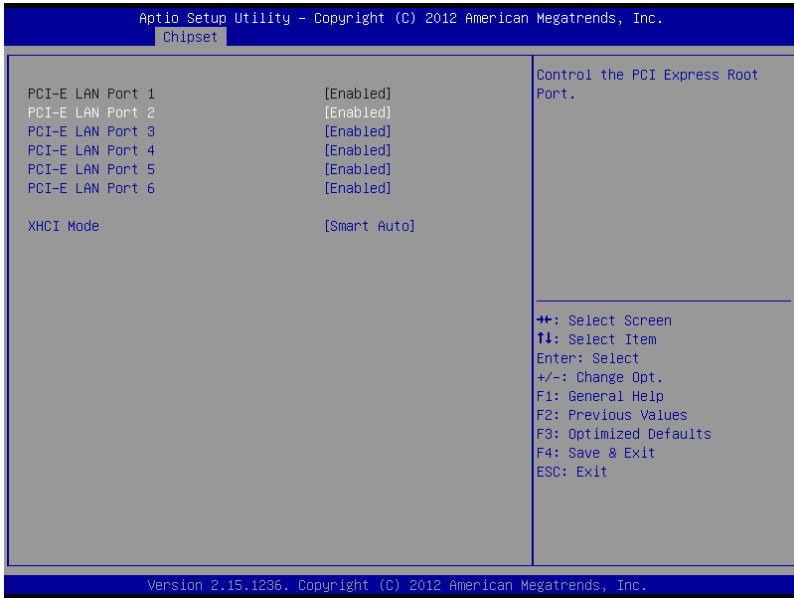
Options summary:

STATUS LED CTRL	LED OFF
	RED LED ON
	RED LED BLINK
	RED LED FAST BLINK
	GREEN LED ON
	GREEN LED BLINK
	GREEN LED FAST BLINK
STATUS LED CTRL help.	
LAN kit Power ON	Bypass
	PassTru
Setting LAN kit function behavior when power on.(Bypass/Pass Through)	
LAN kit Power Off	Bypass
	PassTru
Setting LAN kit function behavior when power off.(Bypass/Pass Through)	
WDT	Bypass
	Reset
WDT function select, Reset: Reset System. Bypass: Reset LAN kits to Bypass mode.	

3.5 Setup submenu: Chipset



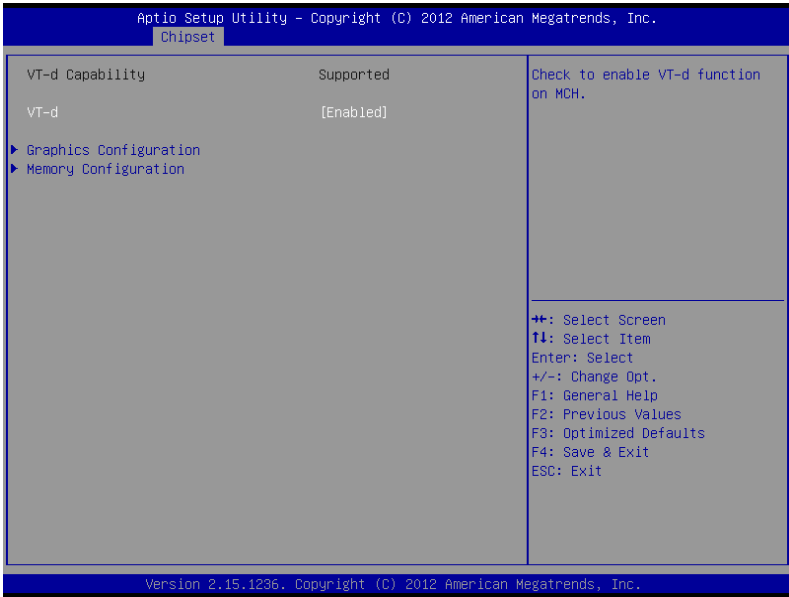
3.5.1 Chipset: PCH-IO Configuration



Options summary:

PCI-E LAN Port n	Disabled
	Enabled
Control the PCI Express Root Port.	
XHCI Mode	Smart Auto
	Auto
	Enabled
	Disabled
Mode of operation of xHCI controller.	Manual

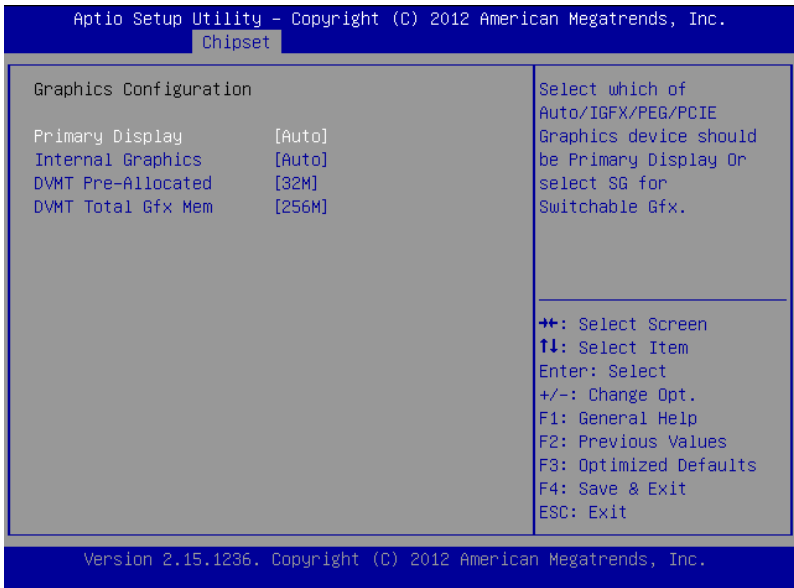
3.5.2 Chipset: System Agent (SA) Configuration



Options summary:

VT-d	Disabled
	Enabled
Check to enable VT-d function on MCH.	

3.5.2.1 System Agent (SA) Configuration: Graphics Configuration



Options summary :

Primary Display	Auto
	IGFX
	PEG
	PCIE
Select which of Auto/IGFX/PEG/PCIE Graphics device should be Primary Display Or select SG for Switchable Gfx.	
Internal Graphics	Auto
	Disabled
	Enabled
Keep IGD enabled based on the setup options.	
DVMT Pre-Allocated	32M
	64M
	96M
	128M
	160M
	192M
	224M

	256M
	288M
	320M
	352M
	384M
Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory Size used by the Internal Graphics Device.	
DVMT Total Gfx Mem	128M
	256M
	MAX
Select DVMT 5.0 Total Graphics Memory Size used by the Internal Graphics Device.	

3.5.2.2 System Agent (SA) Configuration: Memory Configuration

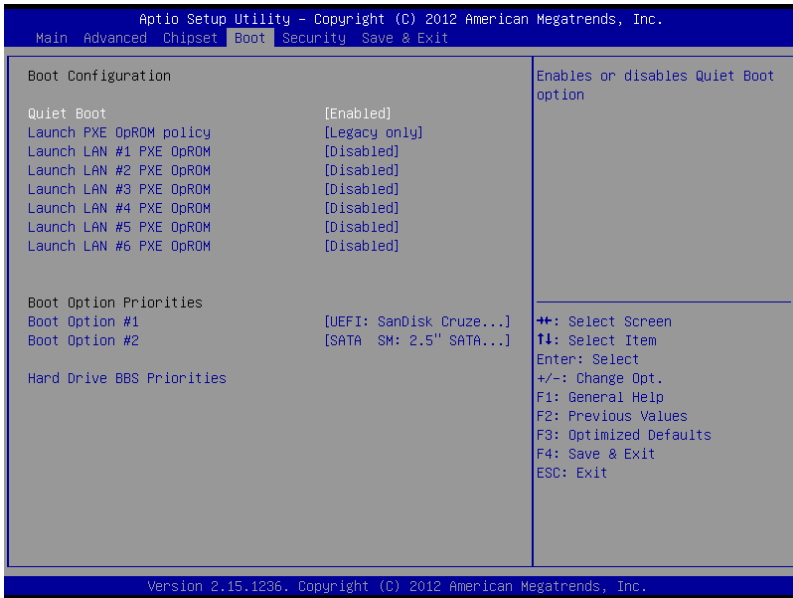
Aptio Setup Utility - Copyright (C) 2012 American Megatrends, Inc.
Chipset

Memory Information	
Memory RC Version	1.8.0.0
Memory Frequency	1600 Mhz
Total Memory	8192 MB (DDR3)
DIMM#0	Not Present
DIMM#1	Not Present
DIMM#2	8192 MB (DDR3)
DIMM#3	Not Present
CAS Latency (tCL)	11
Minimum delay time	
CAS to RAS (tRCDm)	11
Row Precharge (tR)	11
Active to Prechar	28
XMP Profile 1	Not Supported
XMP Profile 2	Not Supported

++: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit

Version 2.15.1236. Copyright (C) 2012 American Megatrends, Inc.

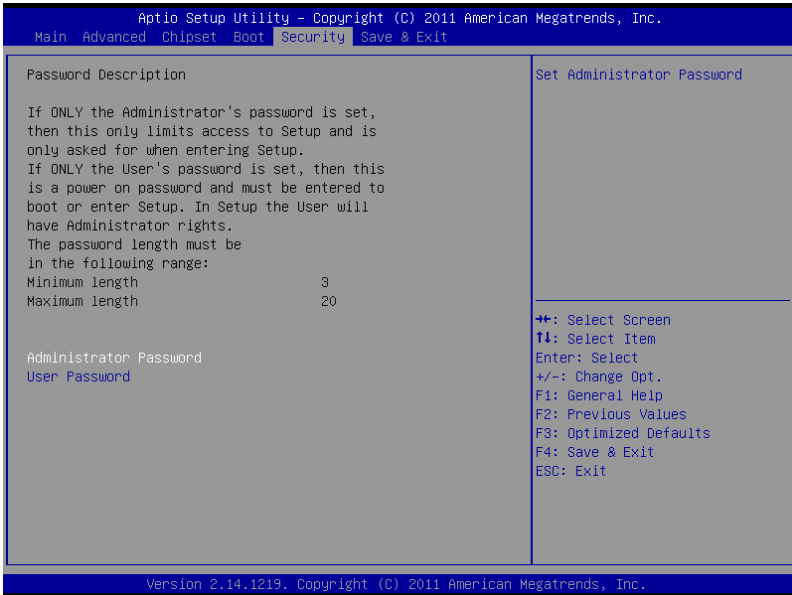
3.6 Setup submenu: Boot



Options summary:

Quiet Boot	Disabled
	Enabled
Enables or disables Quiet Boot option.	
Launch PXE OpROM policy	DO not launch
	Legacy only
Controls the execution of UEFI and Legacy PXE OpROM	
Launch LAN #1~6 PXE OpR	Disabled
	Enabled
Enable or Disable Legacy Boot Option for LAN #1~6 .	

3.7 Setup submenu: Security



Change User/Administrator Password

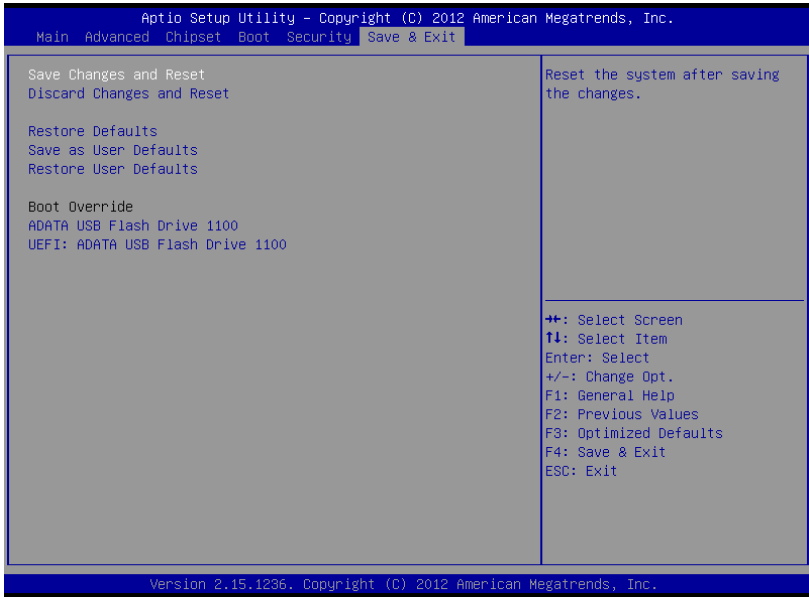
You can set a User Password once an Administrator Password is set. The password will be required during boot up, or when the user enters the Setup utility. Please Note that a User Password does not provide access to many of the features in the Setup utility.

Select the password you wish to set, press Enter to open a dialog box to enter your password (you can enter no more than six letters or numbers). Press Enter to confirm your entry, after which you will be prompted to retype your password for a final confirmation. Press Enter again after you have retyped it correctly.

Removing the Password

Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection.

3.8 Setup submenu: Save & Exit



Chapter 4

Drivers Installation

4.1 Drivers Installation

The drivers can be found in the product page for FWS-7400 at aaeon.com. Please follow the sequence below to install the drivers.

Step 1 – Install Chipset Drivers

1. Open the **Step 1 - Chipset** folder followed by the **iINF_allOS_9.4.0.1027.exe** file
2. Follow the instructions
3. Drivers will be installed automatically

Step 2 – Install VGA Driver

1. Open the **Step 2 - VGA** folder and select your OS
2. Open the **Setup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 3 – Install USB3.0 Drivers

1. Open the **Step 3 – USB3.0** folder followed by the **Setup.exe** file
2. Follow the instructions
3. Drivers will be installed automatically

Step 4 – Install LAN Driver

1. Open the **Step 4 - LAN** folder and select your OS
2. Open the **Autorun.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 5 – Install ME Drivers

1. Open the **Step 5 - ME** folder followed by the **Setup.exe** file
2. Follow the instructions
3. Drivers will be installed automatically

Step 6 – Install IRST Drivers

1. Open the **Step 5 - IRST** folder followed by the **Setup.exe** file
2. Follow the instructions
3. Drivers will be installed automatically

Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Initial Program

Table 1 : SuperIO relative register table		
	Default Value	Note
Index	0x2E(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2 : Watchdog relative register table					
	LDN	Register	BitNum	Value	Note
Timer Counter	0x07(Note3)	0x73(Note4)		(Note24)	Time of watchdog timer (0~255) This register is byte access
Counting Unit	0x07(Note5)	0x72(Note6)	7(Note7)	1(Note8)	Select time unit. 1: second 0: minute
Watchdog Enable (KRST)	0x07(Note9)	0x72(Note10)	4(Note11)	1(Note12)	0: Disable 1: Enable
Timeout Status	0x07(Note13)	0x71(Note14)	0(Note15)	1	1: Clear timeout status

```
*****
// SuperIO relative definition (Please reference to Table 1)
#define byte   SIOIndex //This parameter is represented from Note1
#define byte   SIOData  //This parameter is represented from Note2
#define void   IOWriteByte(byte IOPort, byte Value);
#define byte   IOReadByte(byte IOPort);
// Watch Dog relative definition (Please reference to Table 2)
#define byte   TimerLDN //This parameter is represented from Note3
#define byte   TimerReg //This parameter is represented from Note4
#define byte   TimerVal // This parameter is represented from Note24
#define byte   UnitLDN //This parameter is represented from Note5
#define byte   UnitReg //This parameter is represented from Note6
#define byte   UnitBit //This parameter is represented from Note7
#define byte   UnitVal //This parameter is represented from Note8
#define byte   EnableLDN //This parameter is represented from Note9
#define byte   EnableReg //This parameter is represented from Note10
#define byte   EnableBit //This parameter is represented from Note11
#define byte   EnableVal //This parameter is represented from Note12
#define byte   StatusLDN // This parameter is represented from Note13
#define byte   StatusReg // This parameter is represented from Note14
#define byte   StatusBit // This parameter is represented from Note15
*****
```

```
*****  
VOID Main(){  
    // Procedure : AaeonWDTConfig  
    // (byte)Timer : Time of WDT timer.(0x00~0xFF)  
    // (boolean)Unit : Select time unit(0: second, 1: minute).  
    AaeonWDTConfig();  
  
    // Procedure : AaeonWDTEnable  
    // This procedure will enable the WDT counting.  
    AaeonWDTEnable();  
}  
*****
```

```
*****
// Procedure : AaeonWDTEnable
VOID  AaeonWDTEnable (){
    WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 1);
}

// Procedure : AaeonWDTConfig
VOID  AaeonWDTConfig (){
    // Disable WDT counting
    WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0);
    // Clear Watchdog Timeout Status
    WDTClearTimeoutStatus();
    // WDT relative parameter setting
    WDTParameterSetting();
}

VOID  WDTEnableDisable(byte LDN, byte Register, byte BitNum, byte Value){
    SIOBitSet(LDN, Register, BitNum, Value);
}

VOID  WDTParameterSetting(){
    // Watchdog Timer counter setting
    SIOByteSet(TimerLDN, TimerReg, TimerVal);
    // WDT counting unit setting
    SIOBitSet(UnitLDN, UnitReg, UnitBit, UnitVal);
}

VOID  WDTClearTimeoutStatus(){
    SIOBitSet(StatusLDN, StatusReg, StatusBit, 1);
}
*****
```

```
*****
VOID  SIOEnterMBPnPMode0{
    Switch(SIOIndex){
        Case 0x2E:
            IOWriteByte(SIOIndex, 0x87);
            IOWriteByte(SIOIndex, 0x01);
            IOWriteByte(SIOIndex, 0x55);
            IOWriteByte(SIOIndex, 0x55);
            Break;
        Case 0x4E:
            IOWriteByte(SIOIndex, 0x87);
            IOWriteByte(SIOIndex, 0x01);
            IOWriteByte(SIOIndex, 0x55);
            IOWriteByte(SIOIndex, 0xAA);
            Break;
    }
}

VOID  SIOExitMBPnPMode0{
    IOWriteByte(SIOIndex, 0x02);
    IOWriteByte(SIOData, 0x02);
}

VOID  SIOSelectLDN(byte LDN){
    IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
    IOWriteByte(SIOData, LDN);
}
*****
```

```
*****
VOID  SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
    Byte TmpValue;

    SIOEnterMBPnPMode();
    SIOSelectLDN(byte LDN);
    IOWriteByte(SIOIndex, Register);
    TmpValue = IOReadByte(SIOData);
    TmpValue &= ~(1 << BitNum);
    TmpValue |= (Value << BitNum);
    IOWriteByte(SIOData, TmpValue);
    SIOExitMBPnPMode();
}

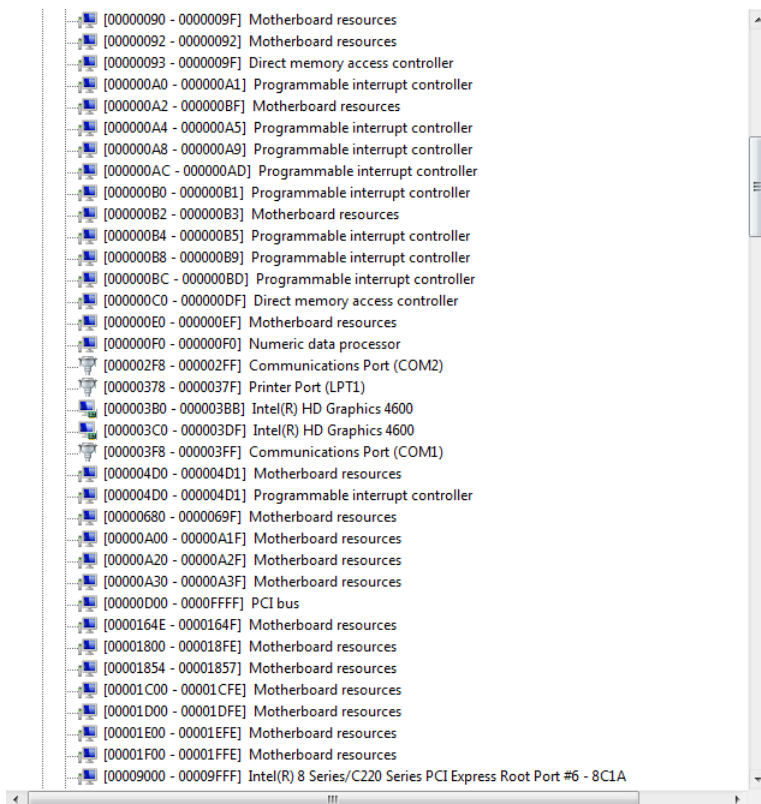
VOID  SIOByteSet(byte LDN, byte Register, byte Value){
    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, Register);
    IOWriteByte(SIOData, Value);
    SIOExitMBPnPMode();
}
*****
```

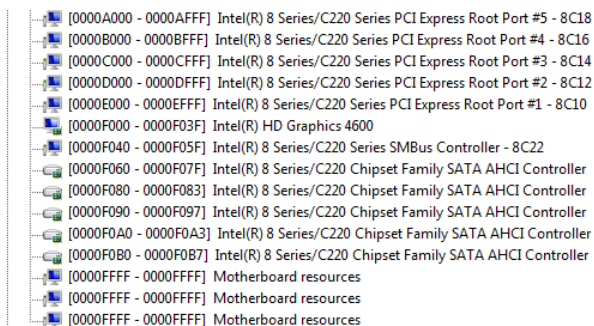
Appendix B

I/O Information

B.1 I/O Address Map

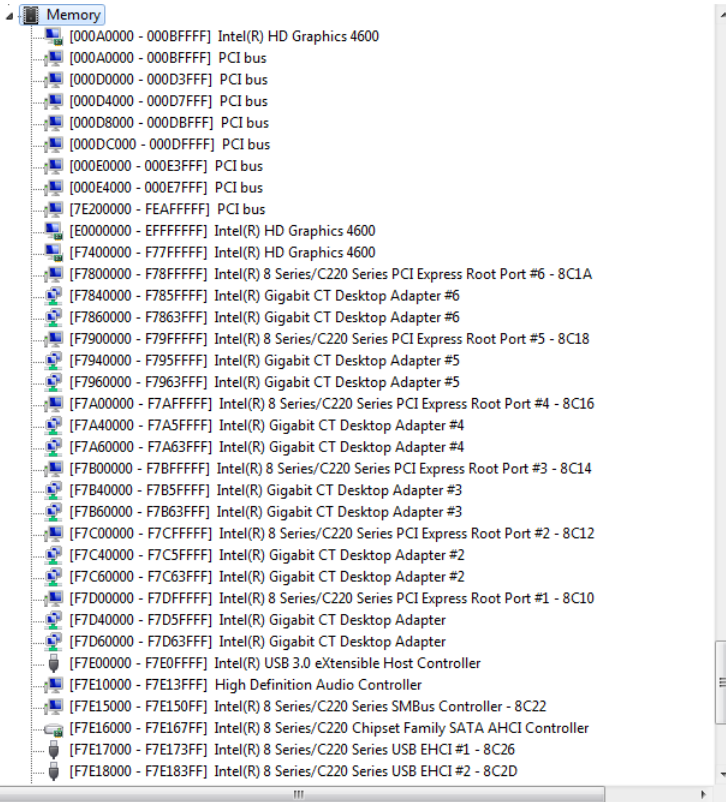
Address Range	Component
[00000000 - 0000001F]	Direct memory access controller
[00000000 - 00000CF7]	PCI bus
[00000010 - 0000001F]	Motherboard resources
[00000020 - 00000021]	Programmable interrupt controller
[00000022 - 0000003F]	Motherboard resources
[00000024 - 00000025]	Programmable interrupt controller
[00000028 - 00000029]	Programmable interrupt controller
[0000002C - 0000002D]	Programmable interrupt controller
[0000002E - 0000002F]	Motherboard resources
[00000030 - 00000031]	Programmable interrupt controller
[00000034 - 00000035]	Programmable interrupt controller
[00000038 - 00000039]	Programmable interrupt controller
[0000003C - 0000003D]	Programmable interrupt controller
[00000040 - 00000043]	System timer
[00000044 - 0000005F]	Motherboard resources
[0000004E - 0000004F]	Motherboard resources
[00000050 - 00000053]	System timer
[00000060 - 00000060]	Standard PS/2 Keyboard
[00000061 - 00000061]	Motherboard resources
[00000062 - 00000063]	Motherboard resources
[00000063 - 00000063]	Motherboard resources
[00000063 - 00000063]	Motherboard resources
[00000064 - 00000064]	Standard PS/2 Keyboard
[00000065 - 00000065]	Motherboard resources
[00000065 - 0000006F]	Motherboard resources
[00000067 - 00000067]	Motherboard resources
[00000070 - 00000070]	Motherboard resources
[00000070 - 00000077]	System CMOS/real time clock
[00000072 - 0000007F]	Motherboard resources
[00000080 - 00000080]	Motherboard resources
[00000080 - 00000080]	Motherboard resources
[00000081 - 00000091]	Direct memory access controller
[00000084 - 00000086]	Motherboard resources
[00000088 - 00000088]	Motherboard resources
[0000008C - 0000008E]	Motherboard resources
[00000090 - 0000009F]	Motherboard resources





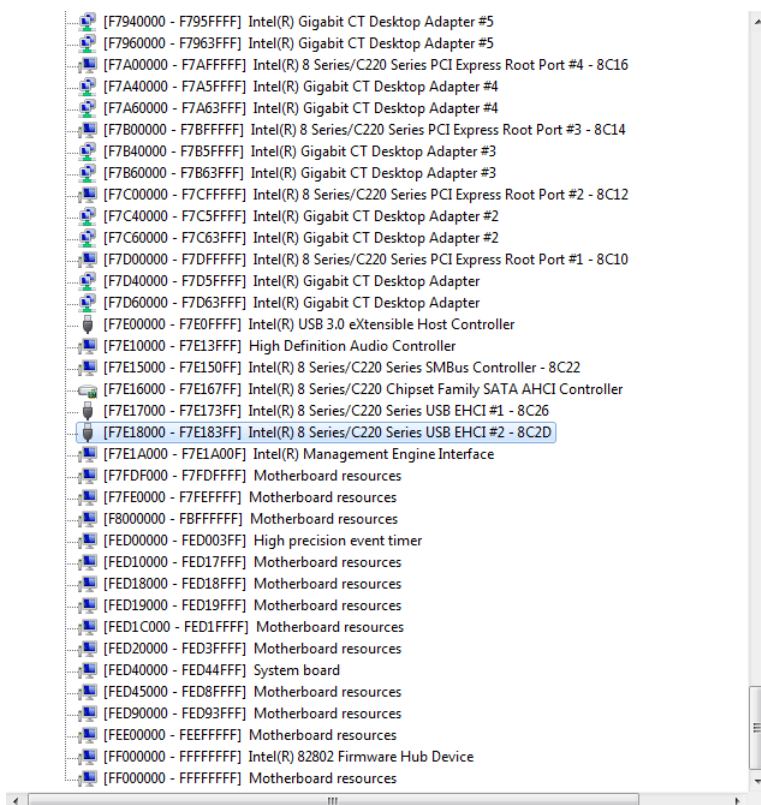
[0000A000 - 0000AFFF]	Intel(R) 8 Series/C220 Series PCI Express Root Port #5 - 8C18
[0000B000 - 0000BFFF]	Intel(R) 8 Series/C220 Series PCI Express Root Port #4 - 8C16
[0000C000 - 0000CFFF]	Intel(R) 8 Series/C220 Series PCI Express Root Port #3 - 8C14
[0000D000 - 0000DFFF]	Intel(R) 8 Series/C220 Series PCI Express Root Port #2 - 8C12
[0000E000 - 0000EFFF]	Intel(R) 8 Series/C220 Series PCI Express Root Port #1 - 8C10
[0000F000 - 0000F03F]	Intel(R) HD Graphics 4600
[0000F040 - 0000F05F]	Intel(R) 8 Series/C220 Series SMBus Controller - 8C22
[0000F060 - 0000F07F]	Intel(R) 8 Series/C220 Chipset Family SATA AHCI Controller
[0000F080 - 0000F083]	Intel(R) 8 Series/C220 Chipset Family SATA AHCI Controller
[0000F090 - 0000F097]	Intel(R) 8 Series/C220 Chipset Family SATA AHCI Controller
[0000FA00 - 0000FAA3]	Intel(R) 8 Series/C220 Chipset Family SATA AHCI Controller
[0000FB00 - 0000FB07]	Intel(R) 8 Series/C220 Chipset Family SATA AHCI Controller
[0000FFFF - 0000FFFF]	Motherboard resources
[0000FFFF - 0000FFFF]	Motherboard resources
[0000FFFF - 0000FFFF]	Motherboard resources

B.2 Memory Address Map

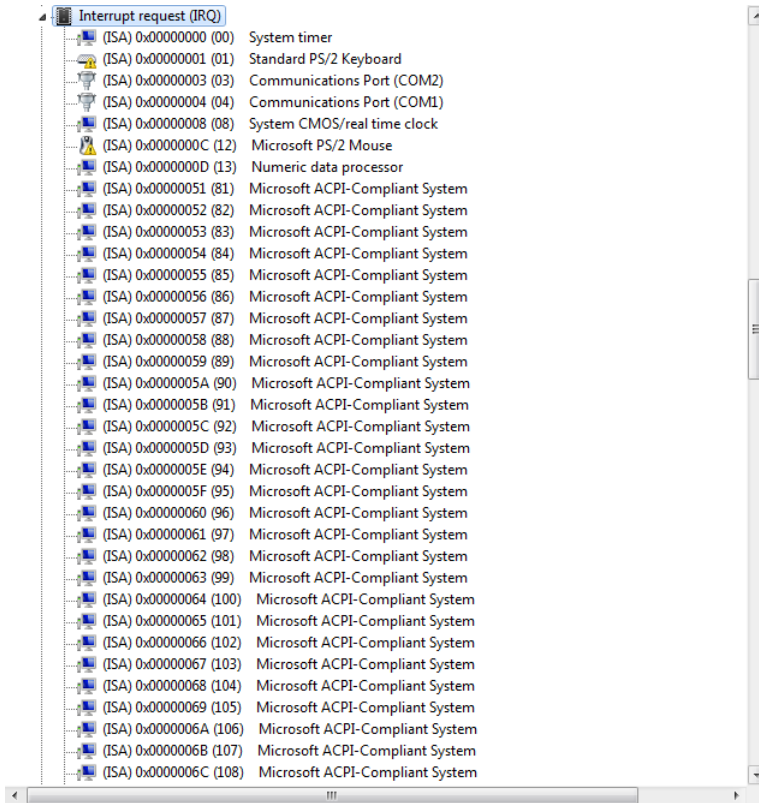


The screenshot shows the 'Memory' section of the Windows System Information tool. It displays a list of memory addresses and their corresponding hardware components. The list includes various Intel(R) HD Graphics 4600, PCI bus, Intel(R) HD Graphics 4600, Intel(R) 8 Series/C220 Series PCI Express Root Port, Intel(R) Gigabit CT Desktop Adapter, Intel(R) 8 Series/C220 Series PCI Express Root Port, Intel(R) Gigabit CT Desktop Adapter, Intel(R) USB 3.0 eXtensible Host Controller, High Definition Audio Controller, Intel(R) 8 Series/C220 Series SMBus Controller, Intel(R) 8 Series/C220 Chipset Family SATA AHCI Controller, Intel(R) 8 Series/C220 Series USB EHCI #1, and Intel(R) 8 Series/C220 Series USB EHCI #2.

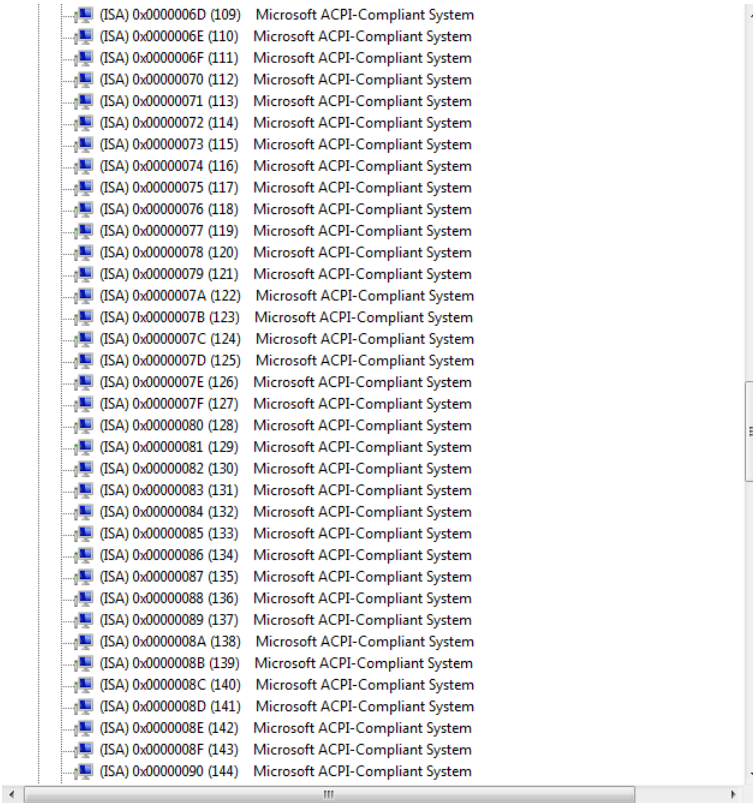
Address	Component
[000A0000 - 000BFFFF]	Intel(R) HD Graphics 4600
[000A0000 - 000BFFFF]	PCI bus
[000D0000 - 000D3FFF]	PCI bus
[000D4000 - 000D7FFF]	PCI bus
[000D8000 - 000DBFFF]	PCI bus
[000DC000 - 000DFFFF]	PCI bus
[000E0000 - 000E3FFF]	PCI bus
[000E4000 - 000E7FFF]	PCI bus
[7E200000 - FEAFFFFF]	PCI bus
[E0000000 - EFFFFFFF]	Intel(R) HD Graphics 4600
[F7400000 - F77FFFFF]	Intel(R) HD Graphics 4600
[F7800000 - F78FFFFF]	Intel(R) 8 Series/C220 Series PCI Express Root Port #6 - 8C1A
[F7840000 - F785FFFF]	Intel(R) Gigabit CT Desktop Adapter #6
[F7860000 - F7863FFF]	Intel(R) Gigabit CT Desktop Adapter #6
[F7900000 - F79FFFFF]	Intel(R) 8 Series/C220 Series PCI Express Root Port #5 - 8C18
[F7940000 - F795FFFF]	Intel(R) Gigabit CT Desktop Adapter #5
[F7960000 - F7963FFF]	Intel(R) Gigabit CT Desktop Adapter #5
[F7A00000 - F7AFFFFF]	Intel(R) 8 Series/C220 Series PCI Express Root Port #4 - 8C16
[F7A40000 - F7A5FFFF]	Intel(R) Gigabit CT Desktop Adapter #4
[F7A60000 - F7A63FFF]	Intel(R) Gigabit CT Desktop Adapter #4
[F7B00000 - F7BFFFFF]	Intel(R) 8 Series/C220 Series PCI Express Root Port #3 - 8C14
[F7B40000 - F7B5FFFF]	Intel(R) Gigabit CT Desktop Adapter #3
[F7B60000 - F7B63FFF]	Intel(R) Gigabit CT Desktop Adapter #3
[F7C00000 - F7CFFFFF]	Intel(R) 8 Series/C220 Series PCI Express Root Port #2 - 8C12
[F7C40000 - F7C5FFFF]	Intel(R) Gigabit CT Desktop Adapter #2
[F7C60000 - F7C63FFF]	Intel(R) Gigabit CT Desktop Adapter #2
[F7D00000 - F7DFFFFF]	Intel(R) 8 Series/C220 Series PCI Express Root Port #1 - 8C10
[F7D40000 - F7D5FFFF]	Intel(R) Gigabit CT Desktop Adapter
[F7D60000 - F7D63FFF]	Intel(R) Gigabit CT Desktop Adapter
[F7E00000 - F7E0FFFF]	Intel(R) USB 3.0 eXtensible Host Controller
[F7E10000 - F7E13FFF]	High Definition Audio Controller
[F7E15000 - F7E150FF]	Intel(R) 8 Series/C220 Series SMBus Controller - 8C22
[F7E16000 - F7E167FF]	Intel(R) 8 Series/C220 Chipset Family SATA AHCI Controller
[F7E17000 - F7E173FF]	Intel(R) 8 Series/C220 Series USB EHCI #1 - 8C26
[F7E18000 - F7E183FF]	Intel(R) 8 Series/C220 Series USB EHCI #2 - 8C2D



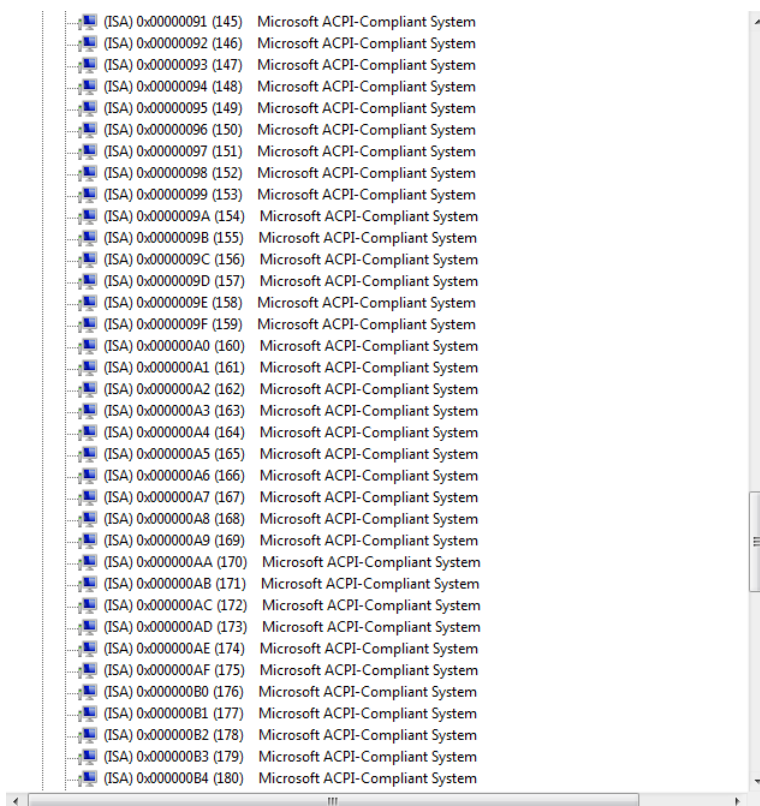
B.3 IRQ Mapping Chart



Device	IRQ
System timer	(00)
Standard PS/2 Keyboard	(01)
Communications Port (COM2)	(03)
Communications Port (COM1)	(04)
System CMOS/real time clock	(08)
Microsoft PS/2 Mouse	(12)
Numeric data processor	(13)
Microsoft ACPI-Compliant System	(81)
Microsoft ACPI-Compliant System	(82)
Microsoft ACPI-Compliant System	(83)
Microsoft ACPI-Compliant System	(84)
Microsoft ACPI-Compliant System	(85)
Microsoft ACPI-Compliant System	(86)
Microsoft ACPI-Compliant System	(87)
Microsoft ACPI-Compliant System	(88)
Microsoft ACPI-Compliant System	(89)
Microsoft ACPI-Compliant System	(90)
Microsoft ACPI-Compliant System	(91)
Microsoft ACPI-Compliant System	(92)
Microsoft ACPI-Compliant System	(93)
Microsoft ACPI-Compliant System	(94)
Microsoft ACPI-Compliant System	(95)
Microsoft ACPI-Compliant System	(96)
Microsoft ACPI-Compliant System	(97)
Microsoft ACPI-Compliant System	(98)
Microsoft ACPI-Compliant System	(99)
Microsoft ACPI-Compliant System	(100)
Microsoft ACPI-Compliant System	(101)
Microsoft ACPI-Compliant System	(102)
Microsoft ACPI-Compliant System	(103)
Microsoft ACPI-Compliant System	(104)
Microsoft ACPI-Compliant System	(105)
Microsoft ACPI-Compliant System	(106)
Microsoft ACPI-Compliant System	(107)
Microsoft ACPI-Compliant System	(108)




























(ISA) 0x000006D (109)	Microsoft ACPI-Compliant System
(ISA) 0x000006E (110)	Microsoft ACPI-Compliant System
(ISA) 0x000006F (111)	Microsoft ACPI-Compliant System
(ISA) 0x0000070 (112)	Microsoft ACPI-Compliant System
(ISA) 0x0000071 (113)	Microsoft ACPI-Compliant System
(ISA) 0x0000072 (114)	Microsoft ACPI-Compliant System
(ISA) 0x0000073 (115)	Microsoft ACPI-Compliant System
(ISA) 0x0000074 (116)	Microsoft ACPI-Compliant System
(ISA) 0x0000075 (117)	Microsoft ACPI-Compliant System
(ISA) 0x0000076 (118)	Microsoft ACPI-Compliant System
(ISA) 0x0000077 (119)	Microsoft ACPI-Compliant System
(ISA) 0x0000078 (120)	Microsoft ACPI-Compliant System
(ISA) 0x0000079 (121)	Microsoft ACPI-Compliant System
(ISA) 0x000007A (122)	Microsoft ACPI-Compliant System
(ISA) 0x000007B (123)	Microsoft ACPI-Compliant System
(ISA) 0x000007C (124)	Microsoft ACPI-Compliant System
(ISA) 0x000007D (125)	Microsoft ACPI-Compliant System
(ISA) 0x000007E (126)	Microsoft ACPI-Compliant System
(ISA) 0x000007F (127)	Microsoft ACPI-Compliant System
(ISA) 0x0000080 (128)	Microsoft ACPI-Compliant System
(ISA) 0x0000081 (129)	Microsoft ACPI-Compliant System
(ISA) 0x0000082 (130)	Microsoft ACPI-Compliant System
(ISA) 0x0000083 (131)	Microsoft ACPI-Compliant System
(ISA) 0x0000084 (132)	Microsoft ACPI-Compliant System
(ISA) 0x0000085 (133)	Microsoft ACPI-Compliant System
(ISA) 0x0000086 (134)	Microsoft ACPI-Compliant System
(ISA) 0x0000087 (135)	Microsoft ACPI-Compliant System
(ISA) 0x0000088 (136)	Microsoft ACPI-Compliant System
(ISA) 0x0000089 (137)	Microsoft ACPI-Compliant System
(ISA) 0x000008A (138)	Microsoft ACPI-Compliant System
(ISA) 0x000008B (139)	Microsoft ACPI-Compliant System
(ISA) 0x000008C (140)	Microsoft ACPI-Compliant System
(ISA) 0x000008D (141)	Microsoft ACPI-Compliant System
(ISA) 0x000008E (142)	Microsoft ACPI-Compliant System
(ISA) 0x000008F (143)	Microsoft ACPI-Compliant System
(ISA) 0x0000090 (144)	Microsoft ACPI-Compliant System

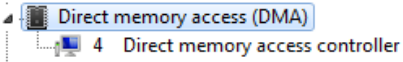


(ISA) 0x00000091 (145)	Microsoft ACPI-Compliant System
(ISA) 0x00000092 (146)	Microsoft ACPI-Compliant System
(ISA) 0x00000093 (147)	Microsoft ACPI-Compliant System
(ISA) 0x00000094 (148)	Microsoft ACPI-Compliant System
(ISA) 0x00000095 (149)	Microsoft ACPI-Compliant System
(ISA) 0x00000096 (150)	Microsoft ACPI-Compliant System
(ISA) 0x00000097 (151)	Microsoft ACPI-Compliant System
(ISA) 0x00000098 (152)	Microsoft ACPI-Compliant System
(ISA) 0x00000099 (153)	Microsoft ACPI-Compliant System
(ISA) 0x0000009A (154)	Microsoft ACPI-Compliant System
(ISA) 0x0000009B (155)	Microsoft ACPI-Compliant System
(ISA) 0x0000009C (156)	Microsoft ACPI-Compliant System
(ISA) 0x0000009D (157)	Microsoft ACPI-Compliant System
(ISA) 0x0000009E (158)	Microsoft ACPI-Compliant System
(ISA) 0x0000009F (159)	Microsoft ACPI-Compliant System
(ISA) 0x000000A0 (160)	Microsoft ACPI-Compliant System
(ISA) 0x000000A1 (161)	Microsoft ACPI-Compliant System
(ISA) 0x000000A2 (162)	Microsoft ACPI-Compliant System
(ISA) 0x000000A3 (163)	Microsoft ACPI-Compliant System
(ISA) 0x000000A4 (164)	Microsoft ACPI-Compliant System
(ISA) 0x000000A5 (165)	Microsoft ACPI-Compliant System
(ISA) 0x000000A6 (166)	Microsoft ACPI-Compliant System
(ISA) 0x000000A7 (167)	Microsoft ACPI-Compliant System
(ISA) 0x000000A8 (168)	Microsoft ACPI-Compliant System
(ISA) 0x000000A9 (169)	Microsoft ACPI-Compliant System
(ISA) 0x000000AA (170)	Microsoft ACPI-Compliant System
(ISA) 0x000000AB (171)	Microsoft ACPI-Compliant System
(ISA) 0x000000AC (172)	Microsoft ACPI-Compliant System
(ISA) 0x000000AD (173)	Microsoft ACPI-Compliant System
(ISA) 0x000000AE (174)	Microsoft ACPI-Compliant System
(ISA) 0x000000AF (175)	Microsoft ACPI-Compliant System
(ISA) 0x000000B0 (176)	Microsoft ACPI-Compliant System
(ISA) 0x000000B1 (177)	Microsoft ACPI-Compliant System
(ISA) 0x000000B2 (178)	Microsoft ACPI-Compliant System
(ISA) 0x000000B3 (179)	Microsoft ACPI-Compliant System
(ISA) 0x000000B4 (180)	Microsoft ACPI-Compliant System

(ISA) 0x000000B5 (181)	Microsoft ACPI-Compliant System
(ISA) 0x000000B6 (182)	Microsoft ACPI-Compliant System
(ISA) 0x000000B7 (183)	Microsoft ACPI-Compliant System
(ISA) 0x000000B8 (184)	Microsoft ACPI-Compliant System
(ISA) 0x000000B9 (185)	Microsoft ACPI-Compliant System
(ISA) 0x000000BA (186)	Microsoft ACPI-Compliant System
(ISA) 0x000000BB (187)	Microsoft ACPI-Compliant System
(ISA) 0x000000BC (188)	Microsoft ACPI-Compliant System
(ISA) 0x000000BD (189)	Microsoft ACPI-Compliant System
(ISA) 0x000000BE (190)	Microsoft ACPI-Compliant System
(PCI) 0x0000000A (10)	Intel(R) 8 Series/C220 Series SMBus Controller - 8C22
(PCI) 0x00000010 (16)	High Definition Audio Controller
(PCI) 0x00000010 (16)	Intel(R) 8 Series/C220 Series USB EHCI #2 - 8C2D
(PCI) 0x00000010 (16)	Intel(R) Management Engine Interface
(PCI) 0x00000017 (23)	Intel(R) 8 Series/C220 Series USB EHCI #1 - 8C26
(PCI) 0xFFFFFD1 (-47)	Intel(R) Gigabit CT Desktop Adapter #6
(PCI) 0xFFFFFD2 (-46)	Intel(R) Gigabit CT Desktop Adapter #6
(PCI) 0xFFFFFD3 (-45)	Intel(R) Gigabit CT Desktop Adapter #6
(PCI) 0xFFFFFD4 (-44)	Intel(R) Gigabit CT Desktop Adapter #6
(PCI) 0xFFFFFD5 (-43)	Intel(R) Gigabit CT Desktop Adapter #6
(PCI) 0xFFFFFD6 (-42)	Intel(R) Gigabit CT Desktop Adapter #6
(PCI) 0xFFFFFD7 (-41)	Intel(R) Gigabit CT Desktop Adapter #5
(PCI) 0xFFFFFD8 (-40)	Intel(R) Gigabit CT Desktop Adapter #5
(PCI) 0xFFFFFD9 (-39)	Intel(R) Gigabit CT Desktop Adapter #5
(PCI) 0xFFFFFDA (-38)	Intel(R) Gigabit CT Desktop Adapter #5
(PCI) 0xFFFFFDB (-37)	Intel(R) Gigabit CT Desktop Adapter #5
(PCI) 0xFFFFFDC (-36)	Intel(R) Gigabit CT Desktop Adapter #5
(PCI) 0xFFFFFDD (-35)	Intel(R) Gigabit CT Desktop Adapter #4
(PCI) 0xFFFFFDE (-34)	Intel(R) Gigabit CT Desktop Adapter #4
(PCI) 0xFFFFFDF (-33)	Intel(R) Gigabit CT Desktop Adapter #4
(PCI) 0xFFFFFE0 (-32)	Intel(R) Gigabit CT Desktop Adapter #4
(PCI) 0xFFFFFE1 (-31)	Intel(R) Gigabit CT Desktop Adapter #4
(PCI) 0xFFFFFE2 (-30)	Intel(R) Gigabit CT Desktop Adapter #4
(PCI) 0xFFFFFE3 (-29)	Intel(R) Gigabit CT Desktop Adapter #3
(PCI) 0xFFFFFE4 (-28)	Intel(R) Gigabit CT Desktop Adapter #3
(PCI) 0xFFFFFE5 (-27)	Intel(R) Gigabit CT Desktop Adapter #3

	(PCI) 0xFFFFFFFF6 (-26)	Intel(R) Gigabit CT Desktop Adapter #3
	(PCI) 0xFFFFFFFF7 (-25)	Intel(R) Gigabit CT Desktop Adapter #3
	(PCI) 0xFFFFFFFF8 (-24)	Intel(R) Gigabit CT Desktop Adapter #3
	(PCI) 0xFFFFFFFF9 (-23)	Intel(R) Gigabit CT Desktop Adapter #2
	(PCI) 0xFFFFFFFFEA (-22)	Intel(R) Gigabit CT Desktop Adapter #2
	(PCI) 0xFFFFFFFFEB (-21)	Intel(R) Gigabit CT Desktop Adapter #2
	(PCI) 0xFFFFFFFFEC (-20)	Intel(R) Gigabit CT Desktop Adapter #2
	(PCI) 0xFFFFFFFFED (-19)	Intel(R) Gigabit CT Desktop Adapter #2
	(PCI) 0xFFFFFFFFEE (-18)	Intel(R) Gigabit CT Desktop Adapter #2
	(PCI) 0xFFFFFFFFEF (-17)	Intel(R) Gigabit CT Desktop Adapter
	(PCI) 0xFFFFFFFFF0 (-16)	Intel(R) Gigabit CT Desktop Adapter
	(PCI) 0xFFFFFFFFF1 (-15)	Intel(R) Gigabit CT Desktop Adapter
	(PCI) 0xFFFFFFFFF2 (-14)	Intel(R) Gigabit CT Desktop Adapter
	(PCI) 0xFFFFFFFFF3 (-13)	Intel(R) Gigabit CT Desktop Adapter
	(PCI) 0xFFFFFFFFF4 (-12)	Intel(R) Gigabit CT Desktop Adapter
	(PCI) 0xFFFFFFFFF5 (-11)	Intel(R) USB 3.0 eXtensible Host Controller
	(PCI) 0xFFFFFFFFF6 (-10)	Intel(R) HD Graphics 4600
	(PCI) 0xFFFFFFFFF7 (-9)	Intel(R) 8 Series/C220 Chipset Family SATA AHCI Controller
	(PCI) 0xFFFFFFFFF8 (-8)	Intel(R) 8 Series/C220 Series PCI Express Root Port #6 - 8C1A
	(PCI) 0xFFFFFFFFF9 (-7)	Intel(R) 8 Series/C220 Series PCI Express Root Port #5 - 8C18
	(PCI) 0xFFFFFFFFFA (-6)	Intel(R) 8 Series/C220 Series PCI Express Root Port #4 - 8C16
	(PCI) 0xFFFFFFFFFB (-5)	Intel(R) 8 Series/C220 Series PCI Express Root Port #3 - 8C14
	(PCI) 0xFFFFFFFFFC (-4)	Intel(R) 8 Series/C220 Series PCI Express Root Port #2 - 8C12
	(PCI) 0xFFFFFFFFFD (-3)	Intel(R) 8 Series/C220 Series PCI Express Root Port #1 - 8C10
	(PCI) 0xFFFFFFFFFE (-2)	Intel(R) Xeon(R) processor E3-1200 v3/4th Gen Core processor PCI Express x16 C

B.4 DMA Channel Assignments



Appendix C

Standard LAN Bypass Platform Setting

C.1 Status LED

The LED status indicator of FWS-7400 is programmable with AAEON SDK for your application.

Table1: LED Status

	STA_LED2	STA_LED1	STA_LED0
LED Off	0	0	0
Red	0	0	1
Red Blinking (Slowly)	0	1	0
Red Blinking (Quickly)	0	1	1
Reserved	1	0	0
Green Blinking (Slowly)	1	0	1
Green Blinking (Quickly)	1	1	0
Green	1	1	1

Table2: Status LED and register mapping table

	Attribute	Register(I/O)	BitNum	Value
STA_LED2	R/W	0xA02(Note1)	5(Note4)	(Note7)
STA_LED1	R/W	0xA02(Note2)	4(Note5)	(Note7)
STA_LED0	R/W	0xA01(Note3)	2(Note5)	(Note7)

Sample Code:

#define Word LED2Add //This parameter is represented from **Note1****#define Word** LED1Add //This parameter is represented from **Note2****#define Word** LED0Add //This parameter is represented from **Note3****#define Byte** LED2Bit //This parameter is represented from **Note4****#define Byte** LED1Bit //This parameter is represented from **Note5****#define Byte** LED0Bit //This parameter is represented from **Note6****#define Byte** UnitVal //This parameter is represented from **Note7**

VOID **SET_Value** (**Word IoAddr, Byte BitNum,Byte Value**){

BYTE TmpValue;

TmpValue = inportb (IoAddr);

TmpValue &= ~(1 << BitNum);

TmpValue |= (Value << BitNum);

outport(IoAddr, TmpValue);

}

VOID **Main**(){\n

SET_Value (LED2Add, LED2Bit, UnitVal); //Setting STA_LED2

SET_Value (LED1Add, LED1Bit, UnitVal); //Setting STA_LED1

SET_Value (LED0Add, LED0Bit, UnitVal); //Setting STA_LED0

}\n

C.2 LAN Bypass

Table1: LAN Kit ID Select

LAN_ID2	LAN_ID1	LAN_ID0	LAN kit selected
0	0	0	LAN Kit 1 Selected
0	0	1	LAN Kit 2 Selected
0	1	0	LAN Kit 3 Selected
0	1	1	LAN Kit 4 Selected
1	0	0	LAN Kit 5 Selected
1	0	1	LAN Kit 6 Selected
1	1	0	LAN Kit 7 Selected
1	1	1	LAN Kit 8 Selected

Table2: LAN Bypass register table

Function	Description
LAN_ID2	Use for selecting which LAN kit will be configured, refer to Table 1 of ID Select table of LAN kit.
LAN_ID1	
LAN_ID0	
PWR_ON	They should be set before ACT_EN. Use for configuring LAN Bypass function behavior to LAN kit, when system power on. 1: Bypass 0: Pass Through
PWR_OFF	Use for configuring LAN Bypass function behavior to LAN kit, when system power off. 1: Bypass 0: Pass Through
WDT_EN	Use for configuring WDT function behavior to LAN kit, when WDT triggered. 0: Normal WDT reset (Default) 1: Force Bypass
ACT_EN	Use for activating programming of LAN kit. It is edge triggering (falling edge 1 to 0) and should be set to high(1) as its normal state.

Table3: LAN Bypass register mapping table

CPLD Slave Address 0x90 (Note1)				
	Attribute	Register(I/O)	BitNum	Value
LAN_ID2	R/W	0xA05(Note1)	7(Note8)	(Note15)
LAN_ID1	R/W	0xA05(Note2)	6(Note9)	(Note15)
LAN_ID0	R/W	0xA00(Note3)	6(Note10)	(Note15)
PWR_ON	R/W	0xA00(Note4)	4(Note11)	(Note15)
PWR_OFF	R/W	0xA00(Note5)	2(Note12)	(Note15)
WDT_EN	R/W	0xA00(Note6)	1(Note13)	(Note15)
ACT_EN	R/W	0xA00(Note7)	5(Note14)	(Note15)

Sample Code

```
*****
#define Word LAN_ID2 //This parameter is represented from Note1
#define Word LAN_ID1 //This parameter is represented from Note2
#define Word LAN_ID0 //This parameter is represented from Note3
#define Byte PWR_ON //This parameter is represented from Note4
#define Byte PWR_OFF //This parameter is represented from Note5
#define Byte WDT_EN //This parameter is represented from Note6
#define Byte ACT_EN //This parameter is represented from Note7
#define Byte LANID2 //This parameter is represented from Note8
#define Byte LANID1 //This parameter is represented from Note9
#define Byte LANID0 //This parameter is represented from Note10
#define Byte PWR_ON_R //This parameter is represented from Note11
#define Byte PWR_OFF_R //This parameter is represented from Note12
#define Byte WDT_EN_R //This parameter is represented from Note13
#define Byte ACT_EN_R //This parameter is represented from Note14
#define Byte UnitVal //This parameter is represented from Note15
*****
```

```

VOID Bypass_Active (Word IoAddr, Byte BitNum){ BYTE TmpValue;
TmpValue = inportb (IoAddr);
TmpValue &= ~(1 << BitNum);
outport(IoAddr, TmpValue);
delay100ms();
TmpValue |= (Value << BitNum);
outport(IoAddr, TmpValue);
}

```

```
*****
```

```

VOID SET_Value (Word IoAddr, Byte BitNum,Byte Value){ BYTE TmpValue;
TmpValue = inportb (IoAddr);
TmpValue &= ~(1 << BitNum);
TmpValue |= (Value << BitNum);
outport(IoAddr, TmpValue);
}

```

```
*****
```

```

VOID Main() {
//Select LAN kit refer to table 1
SET_Value (LAN_ID2, LANID2, UnitVal);
SET_Value (LAN_ID1, LANID1, UnitVal);
SET_Value (LAN_ID0, LANID1, UnitVal);
//Set the PWR_ON parameter
SET_Value (PWR_ON, PWR_ON_R, UnitVal);
//Set the PWR_OFF parameter
SET_Value (PWR_OFF, PWR_OFF_R, UnitVal);
//Set the WDT_EN parameter
SET_Value (PWR_OFF, PWR_OFF_R, UnitVal);
}

```



```
//Active LAN Bypass setting
```

```
Bypass_Active (ACT_EN, ACT_EN_R);
```

```
}
```

```
*****
```

C.3 LCD Module

FWS-7400 provides a LCM (LCD Module) to display information via standard parallel port. User is able to program the LCM to express different status.

Sample Code

```
void Display_Clear()
{
    outportb(0x378, 0x01);
    wait();
    outportb(0x37A, 0xC8);
    wait();
    outportb(0x37A, 0xCA);
    wait();
}

void Return_Home()
{
    outportb(0x378, 0x02);
    wait();
    outportb(0x37A, 0xC8);
    wait();
    outportb(0x37A, 0xCA);
    wait();
}

void Entry_mode_set()
{
    outportb(0x378, 0x06);
    wait();
```

```
outportb(0x37A, 0xC8);
wait();
outportb(0x37A, 0xCA);
wait();
}

void Display_Off()
{
outportb(0x378, 0x08);
wait();
outportb(0x37A, 0xC8);
wait();
outportb(0x37A, 0xCA);
wait();
}

void Display_On_Cursor_Off()
{
outportb(0x378, 0x0C);
wait();
outportb(0x37A, 0xC8);
wait();
outportb(0x37A, 0xCA);
wait();
}

void Display_On_Cursor_On()
{
outportb(0x378, 0x0E);
wait();
```

```
outportb(0x37A, 0xC8);  
wait();  
outportb(0x37A, 0xCA);  
wait();  
}
```

C.4 Software Reset button (General Propose Input)

FWS-7400 provides a general propose input button which status can get by AAEON SDK.

Soft Reset Button Configuration

Table 2: LAN Bypass relative register table

Function	Description
BTN_STS	Reading this register returns the pin level status which is normal high active low. 0: Pin Level States Low. 1: Pin Level States High.

Table 1 : Soft Reset Button register mapping table

	Attribute	Register(I/O)	BitNum	Value
BTN_STS	R	0xA05(Note1)	4(Note2)	(Note3)

Sample Code

```
*****
#define Word BTN_STS //This parameter is represented from Note1
#define Byte BTN_STS_R //This parameter is represented from Note2
*****
Byte GET_Value (Word IoAddr, Byte BitNum,Byte Value){ BYTE TmpValue;
TmpValue = inportb (IoAddr);
    return (TmpValue & (1 << BitNum))
}
*****
```

```
VOID Main() {
```

```
Byte RstBtn;
```

```
RstBtn = GET_Value (BTN_STS, BTN_STS_R); // Active Low
```

```
}
```

```
*****
```